Transients in VSC-HVDC due to control and cell failure

W. Z. El-Khatib, J. Holboell, T. W. Rasmussen

Abstract— **The increasing popularity of High Voltage direct current (HVDC) based on Voltage source converters (VSC) has made it necessary to investigate the behaviour of high power converters under various fault conditions. In this paper we will deal with the transient characteristics of a modular multilevel converter (MMC). Specifically transients evoked due to faults in the converter arms particularly at cell level. Hence a model of a 5-level MMC has to be designed, to give an overview of the impact of transients etc. The functionality of the model is demonstrated by application to a HVDC transmission.**
Detailed knowledge and understanding of the characteristics and behaviour of all relevant power system components under all conditions, including under transients, are required in order to develop reliable transmission system employing HVDC. In the present study, a back to back HVDC transmission system is designed in PSCAD/EMTDC. Simulations and results showing the importance transients analyses are presented.

Keywords: ***Modular multilevel converter, High frequency modeling, High voltage direct current (HVDC) transmission, Electromagnetic transients (EMT) simulation,***

I. INTRODUCTION

THE use of HVDC transmission is becoming a natural part of a modern electrical network due to the great advantages it provides[1] specifically in long distance transmission applications[2]. This is specially seen in offshore wind farms. To take advantage of the large offshore wind resources it has shown necessary to construct wind farm at long distances from shore. Hence that the connection between farm and the onshore grid connection point by means of traditional AC-transmission lines becomes proportionally more infeasible as longer the distance is. This is due to the physical limitation of AC- cables, such as high resistive losses in the cables resistances caused by the capacitive current and the voltage stability problems caused by large cable inductances. Consequently this is leaving void, filled by HVDC-based transmission technologies. Furthermore as the cost is becoming comparable with greater distance HVDC is getting attractive as an alternative for wind power transmission. Onshore, HVDC-technology is widely being used to interconnect areas which are non-synchronous, and for bulk hydro power transmission as seen in many Nordic countries. Hence the hydro power resources are located far from the load centres.

On that background, it is getting increasingly important to investigate the transient behaviour of HVDC-systems. For transient investigations in all kinds of power systems, usually high frequent models are necessary and for HVDC, this includes the converters, and, in particular regarding future systems, the more flexible voltage source converters (VSC) are in focus. Due to the VSC's ability to connect large offshore wind power plants to the onshore grid, and furthermore its ability of connecting asynchronous networks, while keeping the stability of the power system[3], it offers the opportunity for an increased integration of a larger share of renewable energy in the power system.

Since R. Marquardt patented in 2002 a new multilevel topology suitable for very high voltage applications [4], many researches about this topology have been carried out. On the next year, A. Lesnicar explained in [5] the fundamental concepts of the Modular Multilevel Converter (MMC) and a control scheme based on space vector PWM. Some years later S. Allebrod compared in [6] this topology with the classical two level converter. S. Bernet's research group has recently published several papers, for instance [7] and [8], in which MMC's circulating currents are analysed and semiconductor losses for this topology are evaluated.

The focus in this work will be on the transient behaviour of the MMC. Specifically the effects of various cell faults due to gate signal errors. A full scale MMC model including all parasitic components suitable for numerical simulations in time domain will shortly be presented. The control will be described and discussed. Even though VSC is a well-known topology, only few modelling approaches seem to be available, especially regarding transients and the related high frequency range. In order to cover the transient and high frequent range, all parasitic components, in particular of capacitive character had to be added to the model. All contributions are taken into account forming a mathematically and dynamically equivalent, which models the entire converter.

Time domain simulations of a back to back VSC-MMC will demonstrate the performance of the converter in transient conditions. Finally the results of the different fault types will be analysed and discussed.

II. MODULAR MULTILEVEL CONVERTER

The modular multilevel converter is composed of series connected submodules. Each of these submodules consists of 2 IGBTs each with a diode located in anti-parallel and a submodule capacitor as seen from figure-1.

This work was supported in part by the Nordic Energy Research.
W. Z. El-Khatib is with the Technical University of Denmark, CEE, Copenhagen, Denmark (e-mail: wzel@dtu.elektro.dk).
J. Hollbøll is with the Technical University of Denmark, CEE, Copenhagen, Denmark (e-mail: jl@dtu.elektro.dk).
T. W. Rasmussen is with the Technical University of Denmark, CEE, Copenhagen, Denmark (e-mail: twr@dtu.elektro.dk).

Paper submitted to the International Conference on Power Systems Transients (IPST2015) in Zagreb, Croatia June 15-18, 2015.

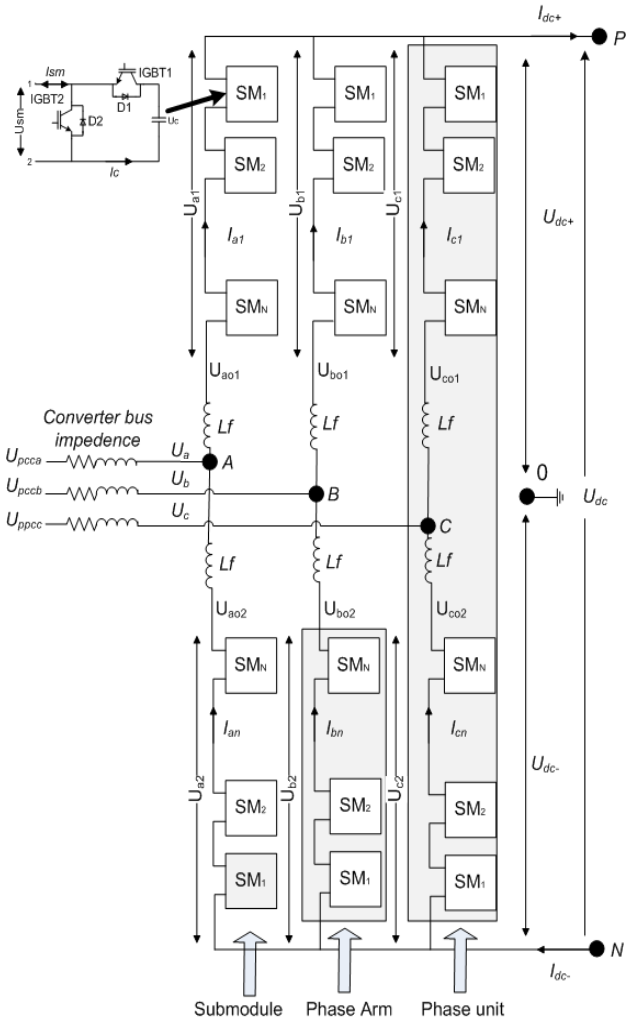

Figure 1 diagram of a three phase Modular Multilevel Converter

The submodule can attain two different states, being either turned on or turned off. Hence working as a controllable voltage source as the submodule changes states.
The DC bus voltage with reference to earth can be expressed as:

$$U_{dc}^{+} = U_{dc}^{-} = \frac{U_{dc}}{2} \tag{1}$$

According to the Kirchhoff's voltage law, the relationship between MMC DC voltage, AC voltage and upper, lower phase arm voltages in figure-1 can be expressed as:

$$U_{k1} = U_{dc}^{+} - U_k = \frac{U_{dc}}{2} - U_k \tag{2}$$

$$U_{k1} = U_{dc}^{-} + U_k = \frac{U_{dc}}{2} + U_k \tag{3}$$

Where $k = a,b,c$. As for the MMC, the amplitude and phase of upper and lower arm voltages (U_{kp} , U_{kn}) are controllable.
The arm voltage with reference to the DC midpoint can be expressed as follows.

$$U_{ko1} = U_{dc}^{+} - \sum_{i=1}^{n} U_{Ci} \cdot (1 - S_i) \tag{4}$$

$$U_{ko2} = U_{dc}^{-} - \sum_{i=1}^{n} U_{Ci} \cdot (S_i) \tag{5}$$

Where the S is the state of the cell and n is the number of cells per arm. From (2) and (3), the DC voltage, U_{dc}, and AC voltage, U_k , could be given by (6) and (7).

$$U_{dc} = U_{kp} + U_{kn} \tag{6}$$

$$U_k = \frac{U_{k1}+U_{k2}}{2} - \frac{U_{dc}^{-}-U_{dc}^{+}}{2} = \frac{U_{k1}+U_{k2}}{2} \tag{7}$$

In a converter applying the MMC-topology, the number of steps of the output voltage is related to the number of series connected submodules and their state, if they are turned on or off. Each phase arm of the MMC consists of a stack which together forms a valve. There are two valves for each phase (e.g. upper and lower). The submodule capacitors are nominally charged to a desired voltage. This means that the output voltage U_k is dependent on the number submodules turned on in each arm. From the equations it becomes clear that when controlling the arm voltages (U_{kp}, U_{kn}) in accordance with equations (2) and (3), the AC voltage phase and amplitude will be controlled accordingly while the DC voltage can be maintained.

$$U_{sm} = \begin{cases} U_c & IGBT1\ ON,\ IGBT2\ OFF \\ 0 & IGBT1\ OFF,\ IGBT2\ ON \end{cases} \tag{8}$$

The definition of the submodule being turned on means that the IGBT called IGBT1 in the figure-2 below is conducting, which means that the current is being conducted through the submodule capacitor. Therefore the voltage across the IGBT called IGBT2, which is turned off, will be the same as the voltage across the submodule capacitor.
When the submodule is turned off, IGBT2 is conducting, and IGBT1 has stopped conducting, therefore the current will be bypassing the submodule capacitor and the submodule will be seen as a short circuit. As a result of this, the voltage across the IGBT2, will be 0.

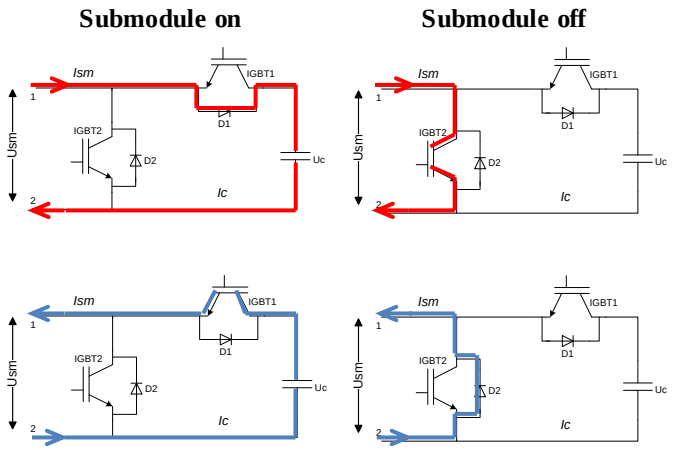

Figure 2:The different operating states of the MMC submodule

Based on the above analysis on submodule operating modes, the cell capacitor current and voltage can be given by (9) and (10).

$$i_c = C\,\frac{dU_c}{dt} \tag{9}$$

$$U_c(t) = U_c(t_0) + \frac{1}{C}\int_{t_0}^{t} I_c(t)\,dt \tag{10}$$

Where $U_c(t_0)$ is the initial capacitor voltage of the submodule, $I_c(t)$ is the current through the capacitor.

Table 1

Parameter	Value	Unit
N (Number of cells per arm)	4	-
P (Active power)	200.0	kW
Q (Reactive power)	0.0	kVar
Fs (switching frequency)	150.0	Hz
U_{dc} (DC voltage)	2000.0	V
U_C (Cell voltage)	500.0	V
C (Cell capacitor)	5600.0	uF
R_{ESR} (Equivalent series resistance)	23.0	mΩ
L_{ESR} (Equivalent series inductance)	20.0	nH
L_{lead} (Equivalent series inductance)	17.2	uH

III. Component Modelling

It is possible to use a simplified method to model the converter [9]. However a full scale model is used to ensure that all system dynamics are included. Furthermore all parasitic components have to be added to clearly see the effects of high frequency transients.

A. Submodule modelling

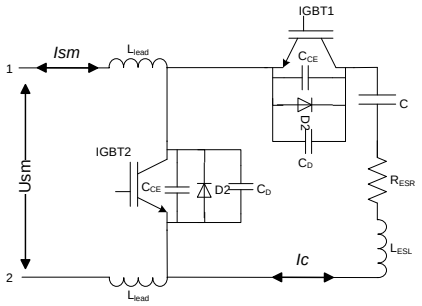

Figure 3 Cell including parasitic components

In the datasheet of any IGBT, usually a number of capacitances are listed. These parasitic capacitances between the terminals of the IGBT are a result of the usage of different semiconductor materiel. For this work we are not considering the optimization of the gate control in addition the sizes of gate-emitter (C_{ge}) and gate-collector (C_{gc}) capacitances in series are negligible compared with collector-emitter (C_{ce}) capacitance, it doesn't contribute to our work to represent them individually, therefore these 3 capacitances have been combined into a single capacitance Figure-3. The capacitances do not have a constants size; in fact there is a highly non-linear relationship between the capacitances and the collector-emitter voltage applied to the IGBT. Besides the capacitances of the IGBT, there will inevitably also be some capacitance across the diode, when not conducting. The submodule capacitor cannot simply be modelled as an ideal capacitor, as this component besides the capacitance also includes some parasitic inductance ESL as well as resistance ESR. The same goes for the terminals of each cell.

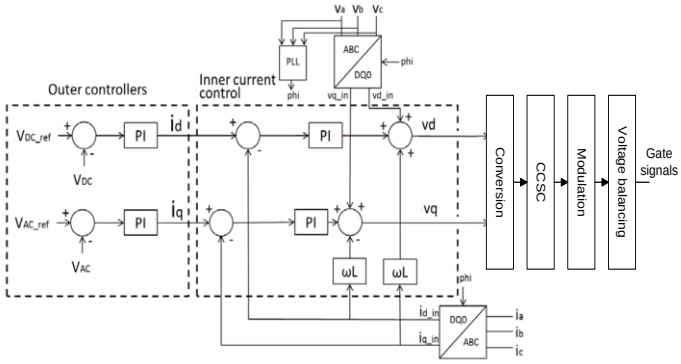

Figure 4 Control strategy for the VSC–MMC station.

A. MMC control system

Given that the MMC topology is a VSC type [10], it uses an upper level control together with an inner controller and an outer controller Figure-4. The MMC model presented in this paper uses the classical vector control strategy that uses the leakage inductance of the transformer and arm inductances to control the current. This method is required to change the current from present value to the reference value [11]. The inner control dq-frame current orders are calculated from active power or DC voltage and reactive powers or AC voltage. In this work the active current order comes from the error between DC voltage and its reference. While the reactive current order is a result of the AC voltage and the reference error. The active and reactive currents in the dq-frame can be independently controlled via a proportional-integral (PI) control [12]. Both the active and reactive power control is used to maintain the voltage within acceptable limits. However, the MMC topology requires additional controllers in order to stabilize internal variables MMC Control; cell capacitor voltages and second harmonic circulating currents of each phase [13].

Voltage unbalances between the arm phases of the MMC introduce circulating currents containing which mainly consists of the second harmonic component which makes the arm current highly asymmetrical and increases the ripple of SM voltages. Circulating currents can be eliminated or reduced by using a low pas filter between the mid-points of the upper and lower arm inductances on each phase [14] or by using an active control over the ac voltage reference coming from upper level control [15]. The MMC model will use the circulating current suppression control (CCSC) [15]. As demonstrated in [16], this control has proved to successfully reduce the second harmonic component of the circulating current significantly and thereby reducing the dc voltage ripple on cell capacitors. The capacitor voltages of all cells must be balanced during normal operation. The cell voltages must be monitored continuously to control the gate signal

according to the balancing control system [17], [18]. The balancing control algorithm [17] requires measurements of all capacitor voltages for every time sample, in order to sort them before selecting the upper and lower cells are being switched on.

IV. Simulation Results

All the simulations shown in this section have been carried out in the software PSCAD/EMTDC. The results obtained by simulating for a three phase MMC with eight submodules in each phase Figure-1. Multiple fault scenarios are simulated and discussed throughout this section. The main simulation parameters are detailed in Table I.

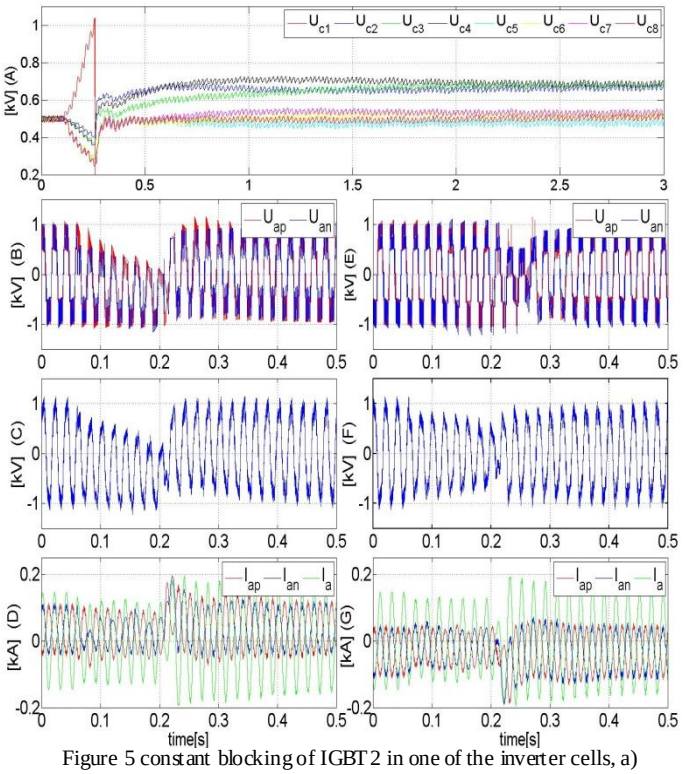

Figure 5 constant blocking of IGBT2 in one of the inverter cells, a) inverter phase cell voltages, b) inverter phase arm output voltages, c) inverter Phase output voltage d), inverter phase arm and output currents, e) rectifier phase Aarm voltages, f) rectifier Phase output voltage, g) rectifier phase arm and output currents.

A. IGBT blocking

Looking at the cell structure it becomes clear that when the lower switch IGBT2 is blocked the only path remaining for positive arm current in the cell is through the cell capacitor. When running the converter in inverter mode the main part of the current is positive Figure-2 upper left. Hence the amplitude of the output current i_k depends on the value of the power while the phase changes when it is transmitting active or reactive power. On the other hand, when P=0 the mean value of the currents i_1 and i_2 is zero whereas if there is a transmission of active power, arm currents present an offset. Consequently the arm current will slowly charge the capacitor Figure-5a. However the arm voltage has to remain equal to the DC voltage $U_{dc} = \sum U_{c,i}$. Thus the voltage in the remaining cells has to be decreased. The decrease in the cell voltages will slowly cause an increasingly asymmetric arm output voltage U_{k1} in accordance to (4) and (5) Figure-5b. To maintain balance between the phase arms the negative arm voltage U_{k2} will also have to be reduced. As a consequence the phase output voltage will become asymmetric as well Figure-5c. The upper arm current i_{k1} will fluctuate while the control is trying to stabilize the arm output voltage. Meanwhile the lower arm current i_{k2} will have larger negative peaks to decrease the cell voltages. During the fault in the inverter, the rectifier will have to reduce the input current to avoid further charging of the DC-link Figure-5g. At some point when the cell voltage in the faulty cell becomes to large either the cell is bypass or the IGBT will breakdown and become a short circuit. Both ways the cell voltage will collapse and the cell will be sidestepped. Nevertheless, thanks to the balancing algorithm explained in [8], in a relatively short time, the remaining cells in the upper arm regulated to $U_{dc}/3$ since there is only 3 cells available. While the lower arm cells are restored to their original condition. These irregularities affect obviously the rest of the system because until these voltages are balanced the sum of them differs from the DC voltage reference. The error produced in this first control loop disestablishes the average current along the phase and consequently the arm currents i_{k1} and i_{k2}. The arm currents in both converters will reach 70% above the normal operation condition.

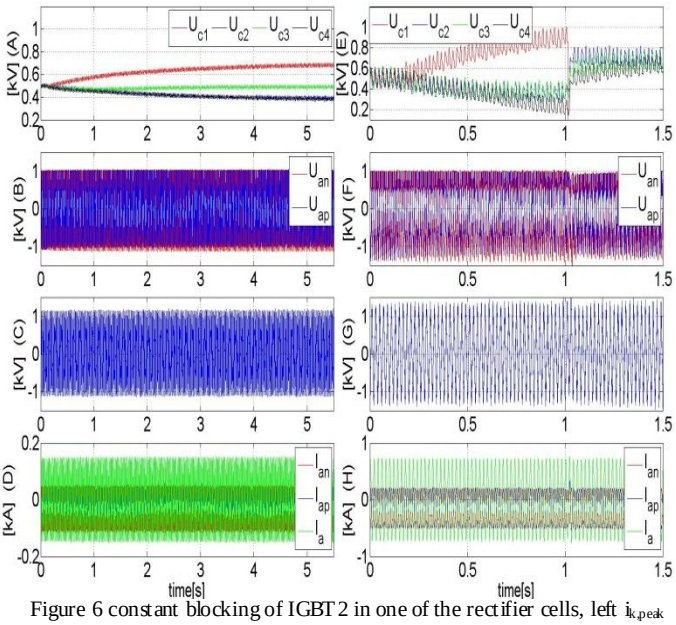

Figure 6 constant blocking of IGBT2 in one of the rectifier cells, left $i_{k,peak}$ =150A , right $i_{k,peak}$ =700A , a,e) rectifier upper arm cell voltages, b,f) rectifier phase arm output voltages, c,g) rectifier Phase output voltage; d,h) rectifier phase arm and output currents.

When blocking IGBT2 in rectifier mode the converter reacts differently from previously. The main reason is; that in rectifier mode the main part of the current is negative (flowing to the DC-link) due to the offset mentioned earlier. Therefore the amount of arm current to charge the cell capacitor is much lower than earlier. As a result of this when the converter is running with an ordered phase peak current of 150A the current is negative for 15ms and positive for the remaining 5ms with peak of 30A. With such conditions the cell capacitor will only be 625V which the capacitor and the IGBT can handle Figure-6a. Hence the rectifier will continue running

with a faulty cell any apparent disturbances on the phase out voltage Figure-6c or current Figure-6d. However increasing the current order to 700A peak will give a 200A positive peak current. Consequently the arm current will charge the faulty cell in the same manner as previously Figure-6e. Nevertheless it should be noted that it takes 5-6 times longer to charge the capacitor even with such a high current. Hence the current is still mainly negative and discharging the capacitor for larger part of the period. Due to the slow charging the converter is able to maintain a stable output within the entire transient period Figure-6g and Figure-6h.

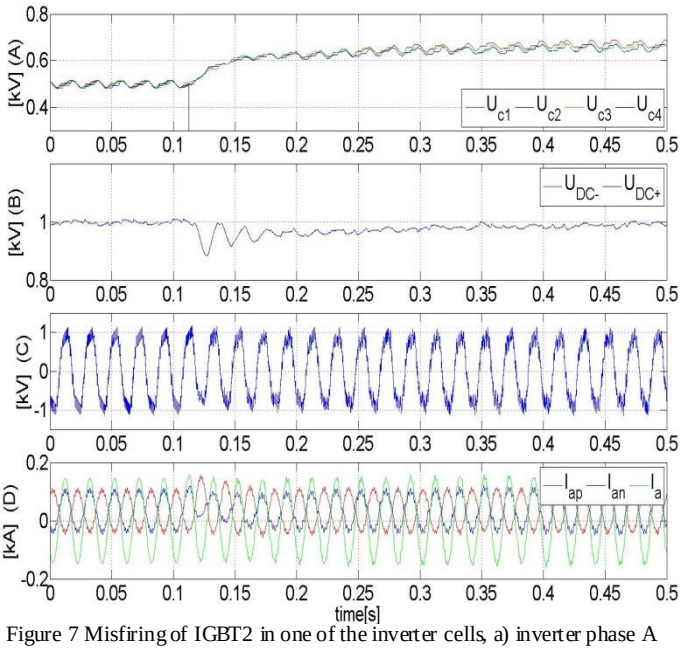

Figure 7 Misfiring of IGBT2 in one of the inverter cells, a) inverter phase A positive arm cell voltages, b) DC-link voltages, c) inverter Phase A output voltage d), inverter phase A arm and output currents

B. IGBT misfiring

In case of any misfiring regardless the converter mode and if it is IGBT1 or IGBT2 the result is more or less the same. If the occurrence happens while the second IGBT is off; the misfired IGBT will conduct current until it is turned off again and the converter will continue operating with none or limited disturbances. However if the second IGBT is on; the result would be a short circuit of the cell capacitor. This will have far more severe consequences. A quick discharge of the capacitor would create a large current that will flow through both IGBT's and properly damaging them both. Nevertheless this discharge will not have an effect on any other components since the current will flow in a closed loop between the positive and negative sides of the capacitor. Obviously such a discharge would cause the cell the cell voltage to collapse rapidly Figure-7a. When the faulty cell is lost the remaining cells will get charged to compensate for the voltage drop in the arm voltage. The charging of the will cause a short 10% oscillation on the DC-link voltage Figure-7b. Looking at the output voltage Figure-7c and currents Figure-7d it is clear that such an event has only small effect on the output.

V. CONCLUSION

Mathematical and dynamical descriptions of modular multilevel converter have been given. The operation of the converter has been explained and equations have been clarified along this article which is valid for any number of cells in the arm.

A high frequent equivalent model for the converter that still maintains the individual identity of every submodule was developed. A control strategy was designed, analysed and shown to work in proper manner. The numerical simulations have shown that the system is operating correctly under steady-state and transient operating conditions. They have also shown that the converter is able to operate correctly during different fault situations even with a low number of cells. Increasing the number of cells will obviously reduce the impact of such faults due to the stress sharing by the cells.

VI. REFERENCES

[1] S. Norrga, "*VSC HVDC-Past, Present and future* " Presentation at the 14th European Conference on Power Electronics and applications, EPE'11(2011) .

[2] K. Friedrich, "*Modern HVDC PLUS Application of VSC in Modular Multilevel Converter Topology",* in: IEEE international Symposium on Industrial Electronic (ISIE), 2010.

[3] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, T. Jonsson, *"VSC-HVDC Transmission with Cascaded Two-Level Converters"*, in: CIGR´E B4-110, 2010.

[4] R. Marquardt, *"Current Rectification Circuit for Voltage Source Inverters with Separate Energy Stores Replaces Phase Blocks with Energy Storing Capacitors,"* German Patent (DE10103031A1), 25 July 2002.

[5] A. Lesnicar, R.Marquardt, *"An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range,"* IEEE Power Tech Conference Proceedings, vol. 3, pp. 6, Bologna 2003.

[6] S. Allebrod, R. Hamerski, R.Marquardt, *"New Transformerless, Scalable Modular Multilevel Converters for HVDC-Transmission,"* IEEE Power Electronics Specialists Conference, pp. 174-179, June 2008

[7] S. Rohner, S. Bernet, M. Hiller, R. Sommer, *"Analysis and Simulation of a 6kV, 6MVA Modular Multilevel Converter,"* IEEE Industrial Electronics Annual Conference, Porto 2009.

[8] S. Bernet, *"Modulation, Losses and Semiconductor Requirements of Modular Multilevel Converter,"* IEEE Transactions on Industrial Electronics, June 2009.

[9] Walid Ziad El-Khatib, Joachim Holbøll, Tonny W. Rasmussen. *"Efficient modeling of modular multilevel converters",* 49 UPEC International Universities' Power Engineering Conference Dublin, Ireland sep. 2013.

[10] L. G. Franquelo et al., *"The age of multilevel converters arrives,"* IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[11] S. Ruihua, C. Zheng, R. Li, and X. Zhou, "VSCs based HVDC and its control strategy," in *Proc. IEEE Transm. Distrib. Conf. Exhibi., Asia Pacific*, Dalian, China, 2005, pp. 1–6.

[12] A. Lindberg, "PWM and control of two and three level high power voltage source converters," Licentiate, Elect. Eng. Dept., Royal Inst. Technol., Stockholm, Sweden, 1995.

[13] A. Antonopoulos, L. Angquist, and H. P. Nee, *"On dynamics and voltage control of the modular multilevel converter,"* 13th Eur. Conference power electron. Appl., Barcelona, Spain oct. 2009

[14] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, *"VSC-HVDC transmission with cascaded two-level converters,"* in Proc. CIGRE Conf., Paris, France, Aug. 2010, pp. B4–110.

[15] S. Ruihua, C. Zheng, R. Li, and X. Zhou, *"VSCs based HVDC and its control strategy,"* in Proc. IEEE Transm. Distrib. Conf. Exhibi., Asia Pacific, Dalian, China, 2005, pp. 1–6.

[16] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, *"Detailed and averaged models for a 401-level MMC-HVDC system,"* IEEE Trans. Power Del., vol. 27, no. 3, pp. 1501–1508, Jul. 2012.

[17] M. Saeedifard and R. Iravani, *"Dynamic performance of a modular multilevel back-to-back HVDC system,"* IEEE Trans. Power Del., vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[18] M. Hagiwara and H. Akagi, *"PWM control and experiment of modular multilevel converter,"* in Proc. IEEE Power Electron. Specialists Conf., Tokyo, Japan, Jun. 2008, pp. 154–161.