

Synchronized Measurement Technology Supported AC and HVDC Online Disturbance Detection

M. Naglic, L. Liu, I. Tyuryukanov, M. Popov, M. A. M. M. van der Meijden, V. Terzija

Abstract—This paper proposes a computationally efficient and robust algorithm for synchronized measurement technology (SMT) supported online disturbance detection. The presented algorithm is based on the robust median absolute deviation (MAD) SMT dispersion measure to locate dataset outlier samples. It can be utilised as a pre-step in alternating current (AC) and high voltage direct current (HVDC) protection schemes. The effectiveness of the proposed algorithm is verified by real-time simulations using a cyber-physical simulation platform, as a co-simulation between the SMT supported electric power system (EPS) model and the underlying information and communications technology (ICT) infrastructure.

Keywords: online disturbance detection, PMU, HVDC, RTDS, co-simulation

I. INTRODUCTION

IN the recent years, the Smart Grid technological advances in terms of sophisticated intelligent electronic devices (IED), fast and reliable telecommunication links, and increased computational capacities have created new opportunities for design of advanced protection schemes.

Typically supported by a global navigation satellite system, the SMT utilizes IEDs with specialized firmware or Phasor Measurement Units (PMU) [1], [2], [3] to deliver time-synchronized wide-area measurements [4] of grid dynamics in real-time. The SMT is the key element of Wide Area Monitoring Protection and Control (WAMPAC) system [5], which is favourable to ensure a higher system stability and reliability.

Nowadays, the HVDC technology is an accepted solution for high capacity power transport. Because of the low impedance of DC cables, the fault penetrates into the HVDC power grid in an extremely fast manner [6]. Without the in-time protection, the fault can lead to the malfunction or break-down of the HVDC and AC grid and considerable economical loss, or in worst case scenario to complete EPS black-out.

Therefore, an adequate disturbance detection has become an important part of EPS protection and refers to the detection of a voltage and current excursion caused by wide variety of electromagnetic phenomena [7]. An important requirement for disturbance detection techniques is to provide online, fast and reliable detection of disturbances that potentially endanger the safe operation of EPS.

A significant amount of work has been done to detect and monitor the EPS operating conditions by leveraging the information extracted from samples of AC grid sinusoidal waveforms. Several approaches were developed based on digital signal processing techniques, mainly wavelet transform [8]-[11], Fourier transform [12], [13], and mathematical morphology [14], [15]. Detection techniques based on S-transform [16], [17] and Kalman filter [18] are also reported in the literature. Authors in [19] perform principal component analysis to detect abnormalities in synchrophasor measurements.

Wavelet transform (WT) based techniques perform well in identifying singularities in signals [20]. In [21], the stationary wavelet transform is applied as a detector of a DC fault, but it requires additional criteria for a reliable detection. The discrete wavelet transform is discussed in [22]; although accurate detection can be ensured, high sampling frequency increases the computation burden. In addition the WTs are noise sensitive, computationally costly and their performances depend on the utilized mother wavelet.

This paper proposes a novel SMT supported online disturbance detection algorithm, which can be utilized as a pre-step of AC and HVDC protection schemes and as an online disturbance monitoring WAMPAC application. The emphasis of the proposed algorithm is on fast response and low computational burden. The algorithm is shown to be capable of detecting large disturbances in AC and HVDC grids, which are seen as sudden deviations in SMT measurements. Large disturbances include but are not limited to switching transients, short circuit faults, line trips and reclosing actions, and large loss of generation or load.

The effectiveness of the proposed algorithm is verified by real-time simulations using a cyber-physical simulation platform as a co-simulation between the SMT supported EPS model and the underlying ICT infrastructure. The test system is a small EPS model that includes an HVDC point-to-point link based on the modular multilevel converter (MMC) technology. The simulations are performed on the RTDS[®] real-time power system simulator with integration of actual SMT components as hardware-in-the-loop (HIL), and online disturbance detection and control center (DDCC) as software-in-the-loop (SIL).

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The aim of this paper is to present the SMT supported online disturbance detection algorithm and its performance capabilities for AC and HVDC. The remaining of the paper is organized as follows: Section II presents data acquisition for AC and HVDC systems. Section III presents the algorithm formulation. Section IV demonstrates the cyber-physical simulation platform and EPS model used. Section V presents the results and discussion. Finally, Section VI concludes the paper.

II. DATA ACQUISITION

In a power system, a voltage or current oscillation signal can be expressed as a sum of complex sinusoidal signals and noise

$$x(t) = \sum_{k=1}^n A_k e^{-\sigma_k t} \cos(\omega_k t + \phi_k) + \varepsilon_k(t) \quad (1)$$

where $n \in \mathbb{N}$ is total number of signal components, A is amplitude, σ is damping ratio, ω is angular frequency, ϕ is phase, and ε represent noise and DC decaying offset of each signal component.

Typically, EPS waveform signals are fed through adequate current and voltage transformers to the waveform input channels of a PMU device [4]. Recently many papers [4], [23], [24] were published about digital signal processing methods for PMU synchrophasor estimation. Through these methods the voltage and current synchrophasors of the fundamental frequency component can be determined from the waveform samples.

In order to extend the proposed algorithm for the disturbance detection on HVDC grids the IEEE C37.118.2 std. messages are exploited as a medium for transferring time-synchronized sampled values. In this case, the DC voltage and current analog signals of appropriate levels are fed directly to the dedicated PMU analog input channels, where signal magnitudes are sampled and transferred in 16-bit integer or IEEE floating-point format [2].

III. METHODOLOGY

It is assumed that in an EPS only the N_b buses of interest are equipped with a PMU device. With m being the number of past measurement samples X_i within the observation time interval, the measurement dataset to be examined of each individual bus i is presented by the following time series vector, also called the sample dataset window W_i .

$$W_i = (X_i[t-m] \dots X_i[t-2] \ X_i[t-1] \ X_i[t]) \quad (2)$$

The proposed disturbance detection algorithm is based on a robust MAD method [25]. The MAD is utilized as a dataset dispersion measure to locate the dataset outlier samples. The MAD is defined by (3) as the median of the absolute deviations from each dataset sample and the median of the complete W_i dataset.

$$MAD = \text{median}(|W_i - \text{median}(W_i)|) \quad (3)$$

Since it is unlikely that the W_i dataset under investigation

has symmetrically distributed sample values, it is prudent to perform the MAD_{double} [26] in order to properly identify the high and low outliers of the dataset. For the MAD_{double} the following pair of statistics first applies

$$\begin{aligned} MAD_{\text{low}} &= \text{median}(|W_i - \text{median}(W_i)|), \ W_i \leq \text{median}(W_i) \\ MAD_{\text{high}} &= \text{median}(|W_i - \text{median}(W_i)|), \ W_i \geq \text{median}(W_i) \end{aligned} \quad (4)$$

where the MAD_{low} value corresponds to the median absolute deviation from the median of all samples less than or equal to the median of the complete W_i dataset, MAD_{high} value corresponds to the median absolute deviation from the median of all samples greater than or equal to the median of the complete W_i dataset.

MAD_{double} therefore represents a combined function of MAD_{low} and MAD_{high} as

$$MAD_{\text{double}}(W_i) = \begin{cases} MAD_{\text{low}}, & W_i \leq \text{median}(W_i) \\ MAD_{\text{high}}, & W_i > \text{median}(W_i) \end{cases} \quad (5)$$

Afterwards, W_{iMAD} , i.e. the MAD-denominated samples of the W_i dataset, are defined as absolute deviations of each dataset sample from the median of the complete W_i dataset, and divided by the corresponding MAD_{double} value as

$$W_{iMAD} = |W_i - \text{median}(W_i)| / MAD_{\text{double}}(W_i) \quad (6)$$

Since W_{iMAD} depends on the whole W_i dataset, consequently it changes after a new measurement sample arrives. Therefore, it is prudent to take into account only the $W_{iMAD}[t]$ most recent sample calculation and save it into $MAD_{\text{save}}[t]$ for further use as:

$$MAD_{\text{save}}[t] = W_{iMAD}[t] \quad (7)$$

In order to determine whether the most recent sample $X_i[t]$ of W_i observation dataset is affected by a disturbance, a dynamic threshold is applied. The dynamic threshold is automatically adjusted based on the $MAD_{\text{save}}[t-1]$ multiplied by the factor of 2, where the threshold is lower bounded by the value of 20 (heuristically determined) in order to prevent false-trigger events in case of small load fluctuations and contingencies. If the following condition is satisfied a disturbance detection trigger ($disturb_{\text{trigger}}$) is set:

$$disturb_{\text{trigger}} = \begin{cases} 1, & MAD_{\text{save}}[t] \geq 2 \cdot MAD_{\text{save}}[t-1] \\ \wedge \quad MAD_{\text{save}}[t] \geq 20 \\ 0, & \text{else} \end{cases} \quad (8)$$

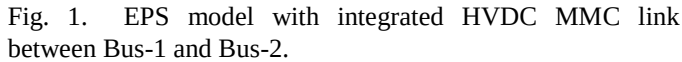
Assuming the application of protection, where a disturbance should be detected as quickly as possible in order to perform required immediate action, the disturbance detection algorithm should operate in an online fashion. Therefore the above presented algorithm is executed every time the W_i dataset is updated with the new most recent SMT measurement.

IV. SIMULATION PLATFORM

In order to demonstrate the performance capabilities of the proposed algorithm the WAMS supported cyber-physical simulation platform [27] is utilized, as a co-simulation

are installed on Bus-1 and Bus-2 using a GTAO card which is used to provide analog current and voltage waveforms. In addition, two PMUs emulated by a GTNETx2 card are installed at Bus-A and Bus-B to deliver time synchronized DC voltage and current values from both HVDC terminal ends. The PMUs are of class P with 50 fps reporting rate. Moreover, to provide accurate time synchronization a GE RT430 grand master clock is used to provide Inter-Range Instrumentation Group code B (IRIG-B) protocol based timestamp and 1 Pulse Per Second (1PPS) time signal to a GTSYNC card and the PMUs. Additionally, the clock provides IEEE 1588 Precision Time Protocol (PTP) time synchronization to a SEL-5073 Phasor Data Concentrator (PDC) and DDCC. Further, the PMU measurements are sent over a WANem telecommunication network emulator (to emulate packet delay, jitter and packet loss) to the PDC, where the measurements are time aligned and forwarded over a local area network (LAN) to the MATLAB based DDCC as presented in Fig. 2. It is important to note that all the platform components are precisely time synchronized to evaluate the time difference (delay) between the disturbance occurrence and its detection.

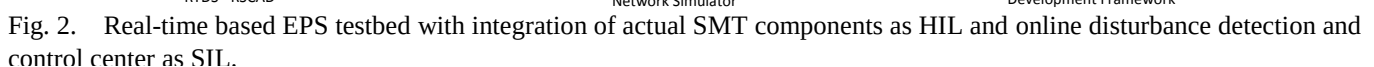
The disturbance detection algorithm is evaluated on the 50 Hz nominal system frequency EPS model (Fig. 1) composed of a generation unit which feeds the load (100 MW) over an MMC-HVDC point-to-point link, installed between Bus-1 and Bus-2.



C. Online synchro-measurement application development framework

The presented EPS model was first implemented in RSCAD and then simulated in real-time using a RTDS[®] power system digital simulator. Furthermore, two physical ALSTOM P847 PMUs with additional OMICRON CMS156 amplifiers

The presented disturbance detection algorithm is implemented using the in-house developed MATLAB supported online Synchro-measurement Application Development Framework (SADF), which is used to design and evaluate SMT supported applications in real-time. The SADF connects to a PDC data stream and parses IEEE



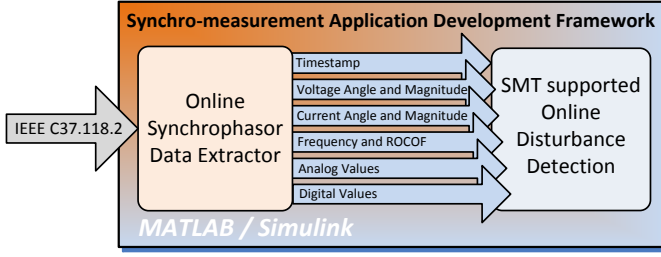


Fig. 3. MATLAB supported Synchro-measurement Application Development Framework.

C37.118.2 [2] type of measurements in online fashion into a user-friendly format in the MATLAB workspace, making it available for the user defined applications (Fig. 3).

In order to perform an adequate control action (i.e. open a circuit breaker to clear the fault), a GTNETx2 SKT socket protocol is used for data exchange between SADF and a RTDS simulated EPS model. Similarly, the control signals are sent over the WANem telecommunication network emulator to emulate packet delay, jitter and packet loss.

The presented platform is suitable for design and performance evaluation of WAMPAC protection and closed-loop corrective control schemes.

V. RESULTS AND DISCUSSION

The proposed algorithm is examined on the benchmark EPS model under different conditions. In general both voltage and current signals can be utilized for disturbance detection. In this paper only the voltage signal is selected as a data source for the disturbance detection since it contains rich indices of system stability. Hereby, the PMU measurements of frequency (typically estimated using voltage angle)/voltage angle and voltage magnitude are utilized in case of AC and HVDC respectively. Moreover, for the AC grid a frequency deviation is required which can be directly determined as a difference between the PMU measured instantaneous and nominal system frequency or with the voltage angle measurements as

$$\Delta f_i|_t = \left(\frac{\theta_{ilt} - \theta_{ilt-\Delta t}}{\Delta t 2\pi} \right) - f_0 \quad (9)$$

where θ_i is the instantaneous angle measurement, f_0 is the nominal system frequency and Δt is the time difference between the samples. The sample dataset window (2) is limited to 50 most recent samples, which corresponds to 1 s of PMU measurements.

A. Platform latency evaluation

The τ_{total} platform latency corresponds to the sum of

$$\tau_{total} = \tau_{PMU} + \tau_{PMU-PDC} + \tau_{PDC} + \tau_{PDC-DDCC} + \tau_{parse} + \tau_{DDCC} \quad (10)$$

where τ_{PMU} is PMU processing delay, $\tau_{PMU-PDC}$ is ICT delay between PMU, WANem and PDC, τ_{PDC} is PDC processing delay, $\tau_{PDC-DDCC}$ is ICT delay between PDC and DDCC, τ_{parse} is IEEE C37.118.2 protocol parsing delay of SADF, τ_{DDCC} is processing delay related to the DDCC disturbance detection algorithm. The approximate platform time delays are presented in Table 1.

TABLE I: PLATFORM DELAYS

Delay Source	Time Range
τ_{PMU}	~ 11 ms
$\tau_{PMU-PDC}$	~ 0.4 ms
τ_{PDC}	~ 0.6 ms
$\tau_{PDC-DDCC}$	~ 0.4 ms
τ_{parse}	~ 0.7 ms per PMU
τ_{DDCC}	~ 0.11 ms per W_{Nb}

B. Self-cleared disturbance detection

The performance capabilities of the proposed algorithm are evaluated on voltage sag disturbances caused by self-cleared phase-to-ground short circuits on Bus-1 and Bus-2 and pole-to-pole and pole-to-ground short circuits on Bus-A and Bus-B, as summarized in Table 2.

TABLE II: STUDY CASES

Grid	Scenario Case	1: Rf=0.001 Ω 2: Rf=10 Ω 3: Rf=100 Ω								
		Fault duration [ms]								
		1	20	100	1	20	100	1	20	100
AC	A: 1P-G@Bus-1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	B: 2P-G@Bus-2	✓	✓	✓	✓	✓	✓	✓	✓	✓
	C: 3P-G@Bus-1	✓	✓	✓	✓	✓	✓	✓	✓	✓
HVDC	D: P-P@Bus-A	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E: P-G@Bus-B	✓	✓	✓	✓	✓	✓	✓	✓	✓

Each case contains additional three scenarios with the varying short circuit resistance and self-clearing fault time. As presented in Table 2, the disturbance was successfully detected on the faulted bus in all the cases. Due to the paper space limitation, only a limited number of simulation results is graphically presented.

1) Case – A, scenario – 1

Fig. 4. presents a single-phase line-to-ground fault with 0.001 ohm resistance, initiated on Bus-1 and self-cleared after 1 ms. The fault occurrence and clearance time are indicated with the red and black stem respectively. The blue line represents frequency deviations on Bus-1, while the orange line represents the corresponding MAD_{save} . The PMU measurement at which the proposed algorithm has identified the disturbance is marked with the green stem while the DDCC disturbance detection time is marked with the blue stem respectively.

As seen from Fig. 4 the disturbance was first detected on Bus-1. Due to the nature of PMU sampling, windowing and measurement timestamping the disturbance affected PMU sample (green stem) seems to detect and report the fault before the fault actually occurred (red stem). This has practical merits since the PMUs estimate the synchrophasors with a two cycles window length with a timestamp corresponding to the time of an observation window centre. Therefore, if the fault affected waveform samples are present in the second half of the synchrophasor estimation window, they also affect the corresponding resulting synchrophasor measurement with the timestamp before the fault actually occurred.

The disturbance caused by the single-phase line-to-ground fault on Bus-1 was successfully detected on all of the disturbance affected buses with the 26.2 ms disturbance detection delay caused by data acquisition and processing.

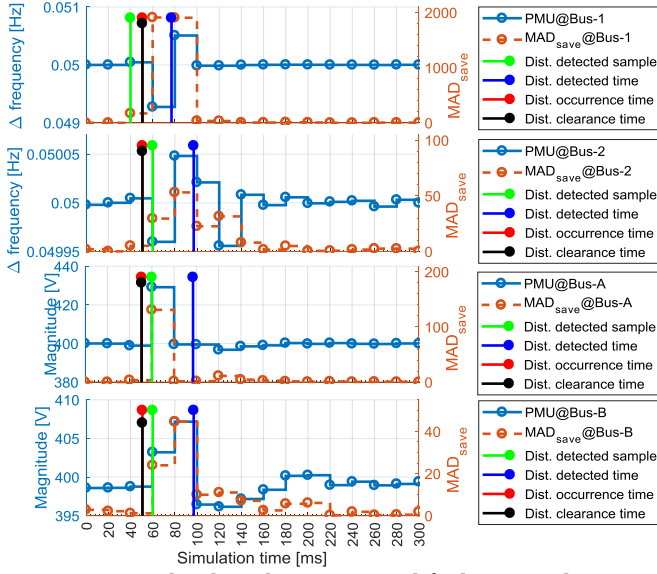


Fig. 4. A single-phase line-to-ground fault initiated on Bus-1 and self-cleared after 1 ms.

2) Case – E, scenario – 3

Fig. 5 presents a pole-to-ground fault with 100 ohm resistance initiated at Bus-B and self-cleared after 1 ms. The disturbance caused by the fault was detected after 9.8 ms of its occurrence first by the PMU placed at Bus-2. As already explained above, the PMU (Bus-2) synchrophasor estimation window contained disturbance affected samples.

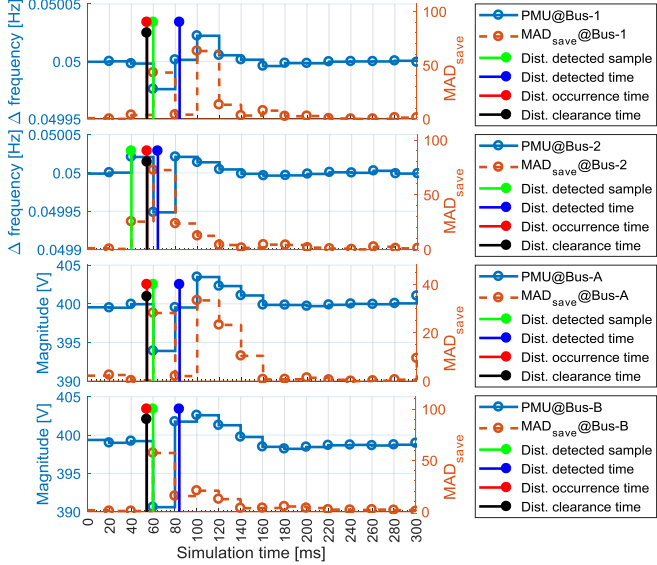


Fig. 5. A pole-to-ground fault, initiated on Bus-B and self-cleared after 1 ms.

The PMUs positioned at Bus-A and Bus-B sampled the analog DC voltage signal at the moment which corresponded to the PMU measurement timestamp. The disturbance imposed by the pole-to-ground fault was detected by the proposed algorithm on all four PMU monitored buses.

3) Case – B, scenario – 3

Fig. 6. represents a two-phase line-to-ground fault with 100 ohm resistance, initiated on Bus-2 and self-cleared after 100 ms. The disturbance was detected with 20.2 ms delay after its occurrence first on Bus-2 and Bus-B.

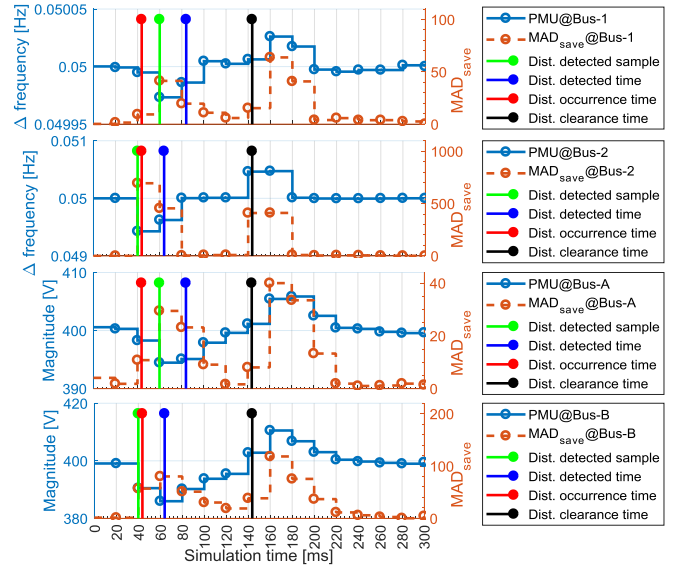


Fig. 6. A two-phase line-to-ground fault initiated on Bus-2 and self-cleared after 100 ms.

4) Case – C, scenario – 3

Fig. 7 presents a tree-phase line-to-ground fault with 100 ohm resistance, initiated on Bus-1 and self-cleared after 20 ms. The disturbance was detected with 14.2 ms delay on the faulted Bus-1. On the remaining buses the disturbance was seen as small perturbations, which were not detected as disturbances due to the lower bounding of the $disturb_{trigger}$.

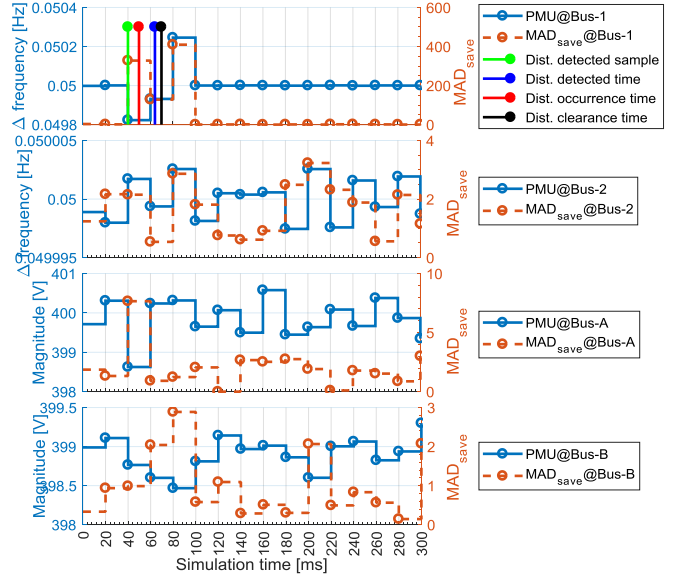


Fig. 7. A tree-phase line-to-ground fault initiated on Bus-1 and self-cleared after 20 ms.

The above presented results demonstrate the effectiveness of the proposed algorithm, which requires only one PMU disturbance-affected measurement sample for an accurate detection. Based on the simulations performed on a typical office personal computer (PC), the disturbance detection algorithm is executed in average 0.11 ms per sample dataset window, while the typical stationary wavelet transform disturbance detection technique (Haar wavelet, level 1 decomposition) requires 1.18 ms. As presented, PMUs can be successfully utilized also for transferring time-synchronized

HVDC grid measurements. The latency between disturbance occurrence and its detection varies typically between 9.8 ms and 32 ms in case no additional packet delay is emulated. It is important to note that fault occurrence moment (relative to PMU observation window centre), PMU synchrophasor estimation algorithm and its measurement reporting rate, ICT data transmission latencies, PDC and DDCC data pre-processing delays are directly related to the response of the proposed disturbance detection algorithm and its performance.

VI. CONCLUSIONS AND FUTURE WORK

This paper proposes a computationally efficient and robust algorithm for SMT supported online disturbance detection, which can be utilized as a standalone WAMPAC application or as a pre-step of AC and HVDC protection schemes. Based on the performed real-time simulations, the proposed algorithm has the following features and superiorities:

- low-complexity of implementation
- fast response and low computational burden
- ability to operate in all types of faults including high-resistance faults with 1 ms duration
- robust to load fluctuations
- applicable for disturbance detection on AC and HVDC grids

Considering the modern small fiber optic telecommunication latencies, the proposed algorithm has practical merits in advanced protection schemes. Further research will be conducted to automatically classify the disturbance.

VII. ACKNOWLEDGMENT

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