Study on Transient Overvoltages in the Converter Station of HVDC-MMC links

H. Saad, P. Rault, S. Dennetière, K. Dudas

***Abstract* – Transient overvoltages in converter station equipment are difficult to predict using analytical tools, therefore it is conducted by means of EMT simulations. To get the worst case values, several HVDC set point configurations (as active/reactive power set points) and fault locations inside the converter station must be simulated. Parametric studies using EMT-type software is conducted, in this paper, to simulate this high number of scenarios. A generic HVDC-MMC link and the impact of arm inductance location are considered. Transient overvoltages at each electrical nodes in the converter station are provided and analyzed. These set of results and studies provide insights for researchers and engineers who are involved in insulation coordination of HVDC-MMC link.**

***Keywords*: Insulation coordination, EMTP, HVDC transmission, MMC, VSC, station faults, switching overvoltage.**

I. Introduction

The inclusion of High Voltage Direct Current (HVDC) transmission link in ac grids is expanding rapidly. The use of voltage source converters (VSCs) based on Modular Multilevel Converter (MMC) topology is becoming more attractive mainly due to their higher performances and lower cost.

During the design phase of a HVDC project, insulation coordination studies is a crucial point for the lifetime of the system and, therefore, should be addressed carefully. In HVDC-MMC link system, if the equipment withstand voltage is chosen to be too high, manufacture of converter equipment can be difficult and will increase the total cost of the system. If the withstand voltage of equipment is chosen to be too low, the failure probability because of malfunction and faults will consequentially increase, causing unavailability of the HVDC link in return.

Therefore, one of the main objective of the insulation coordination studies is to establish the maximum steady-state, temporary and transient voltage levels to which the various components of the system will be exposed [3]. Internal faults in the converter station must be evaluated to determine these maximum overvoltages at each equipment. These maximum overvoltages are difficult to predict using analytical tools, therefore it is conducted by means of EMT simulations. However, to get the worst case value, several HVDC set point configurations (as active/reactive power set points) and fault locations inside the converter station must be simulated. Several articles and research work have been performed on insulation coordination (and fault behavior) of HVDC-LCC link as in [2] and [3]. However, there is only few articles regarding insulation coordination on HVDC-MMC link dealing with internal converter station faults. In [1], an overview on the overvoltages in MMC station is presented and in [5]-[4] studies on transient overvoltages and the impact on the dc cable is performed. In this paper, parametric studies using EMTP-RV software [8] is conducted to simulate this high number of scenarios and to identify the worst case scenario.

Circuit configuration of converter station can vary depending on project specification and manufacturers. The impact of the arm reactor location on equipment stresses is also studied. A generic HVDC-MMC link based on [7] and on the Cigré DC grid benchmark [6] is considered. Overvoltage at each electrical node in the converter station are presented. These set of results and studies are useful for researchers and engineers who are involved in insulation coordination of HVDC-MMC station. XLPE technology is used more and more for HVDC cables projects. The main advantages of XLPE cables compared with Mass Impregnated (MI) and OF (oil-filled) cables are their cost and their environment impact. Nevertheless they are more sensitive to voltage transients and especially polarity reversal [5]. This paper also contributes to a better assessment of transients that can stress DC cables.

The paper is organized as follow: Section II introduces the VSC-HVDC generic model used in this study. Section III describes the parametric test setup considered for running fault transient studies. Section IV displays and analyses the maximal voltage stress on different components, while providing time domain results for relevant situations. Section V analyses the behaviour of the worst case faults. Finally, Section VI resumes the overvoltage study considering DC surge arresters to protect the XLPE cable.

II. HVDC setup

The generic monopolar HVDC point-to-point link based on the Cigré brochure B4-57 [6] and discribed in [7] is considered (Figure 1). The ac grids are presented as equivalent sources with a short-circuit level. The transmission capacity of the link is 1,000 MW. The dc cable is rated ± 320 kV with 200 km lentgh and is modeled using a wideband line model [9]. A MMC 201-level (200 SMs/arm) is considered with a time step of 50 µs. The control strategy considers an active/reactive power flow control on MMC-1 and a dc voltage/reactive power control on MMC-2. Control system details are reported in [6]. In this paper, the protection system has been further developped to trip the link when fault occurs. The considered protections are: AC undervoltages, overcurrent

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on each arm, DC overcurrents and overvoltage on DC terminals.

After fault occurence, the protection system send the trip order, i.e. the converter is blocked and the ac circuit breaker is opened. In order to account for delays between protection system and power circuit equipement, artificial delays are added between the order reception and the action: 200 µs for blocking the MMC and 40 ms for opening the AC circuit breaker (BRK1 and BRK2 in Figure 1) .

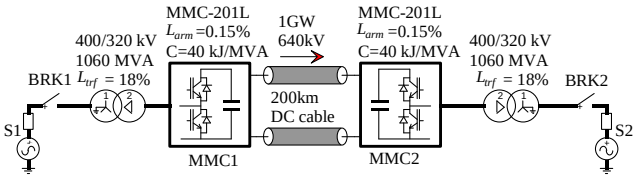


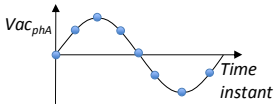
Figure 1: MMC-HVDC transmission system

Accurate MMC model must be used, because internal fault leads to fast dynamic transients. Non-linear IGBT/diodes model are used in the converter model to account for switching surge when MMC blocks [7] and [10].

III. Paremetric Study Setup

To identify the worst case scenario that leads to the maximum transient overvoltage on each converter station equipment, a wide range of scenarios is simulated. Parametric studies are conducted using EMTP-RV software. Maximum active/reactive power transit and solid faults are considered for all scenarios. Parametric studies considers: HVDC active/reactive power transit directions, internal fault types, internal fault instant occurring on the AC point on wave and AC grid short-circuit level (SCL). Table 1 summarizes these parameter variations and the number of configurations. In Figure 2, MMC topology and fault locations are depicted.

Table 1: Setup configuration for parametric study

Parameter	Number of configurations
Fault type	8 configurations see Figure 2: F1 - Phase-to-ground fault F2 - Three phase-to-ground fault F3 - Two phase-to-ground fault F4 - Phase-to-phase fault F5 - Positive arm-to-ground fault F6 - Negative arm-to-ground fault F7 - Positive DC pole-to-ground fault F8 - Negative DC pole-to-ground fault
Fault instant	8 configurations : Fault instant with equal distrubtion at each 2,5 ms 
Transit of active power	2 configurations : ±1000 MW
Transit of reactive power	2 configurations : ±300 MVar
Short circuit level	2 configurations for S1/S2 SCLmax = 50 GVA and SCLmin = 3 GVA

From Table 1, the total number of configurations to be simulated is 512. DC pole-to-pole fault and AC faults on the primary side are not considered since it is expected that such faults will not lead to higher overvoltages on converter equippiment. Metalic faults (i.e. with no impedance) are considered because they intend to generate the worst transients.

For each configuration, absolute maximum peak overvoltage values are measured at each electrical node of the converter station as depicted in Figure 3. The following voltages are: AC primary ($v_{prim_{abc}}$), AC secondary ($v_{\sec_{abc}}$), arm-to-ground ($v^{g}_{u\ell_{abc}}$), arm pole-to-pole ($v_{u\ell_{abc}}$) and DC pole-to-ground (V^{-}_{dc} and V^{+}_{dc}).

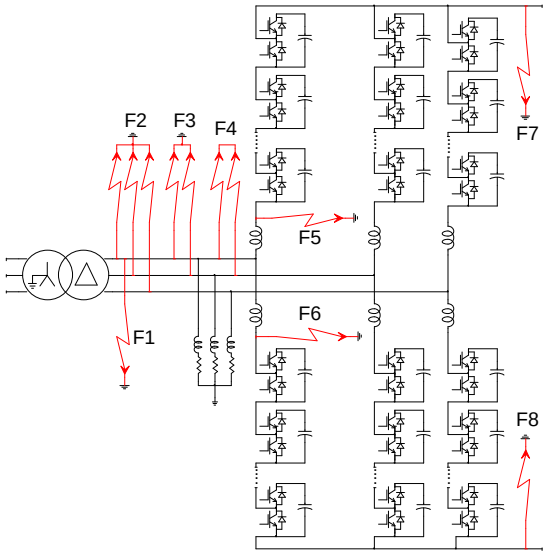


Figure 2: Internal fault locations

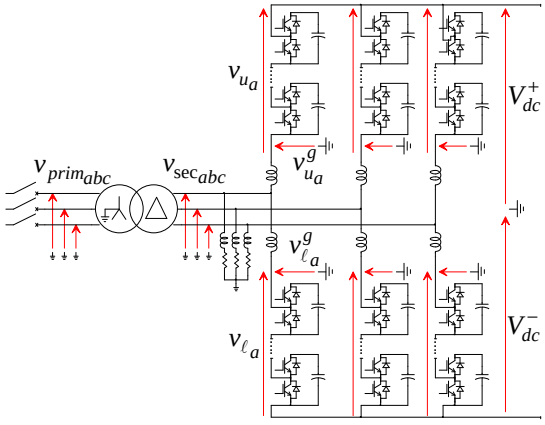


Figure 3: Overvoltage measuring locations

IV. Overvoltage Results

In this section, the EMT parametric studies results are presented and analyzed.

A. Maximum overvoltages without surge arresters

First step, the 512 configurations are simulated in time domain with no surge arresters in order to get the maximum transient overvoltages of the converter station.

1) DC pole-to-ground overvoltage

For the simulated test cases, the maximum peak overvoltage measured at V_{dc}^{-} and V_{dc}^{+} are plotted in Figure 4. The x axis represents the 512 simulated number and the fault types. Whereas, the y axis presents the absolute maximum switching overvoltage peaks registered for each simulated configuration. It is observed that F7 and F8 (i.e. positive and negative DC pole-to-ground faults) represent the worst case scenario that lead to the highest overvoltage values. Nevertheless, F5/F6 lead also to high overvoltages. The maximum switching overvoltage registered is equal to 685 kV. Generally speaking, the configuration of the link, fault instant and SCL have a small impact on this overvoltage. We notice that; high SCL tends to increases the overvoltage in the considered test case. Figure 5 shows the time-domain results of V_{dc}^{+} due to F8 including the impact of SCL and active power transit. It can be noticed, that the configuration -1000 MW/ -300 MVar/ SCLmax leads to the highest overvoltage peak for the considered test case.

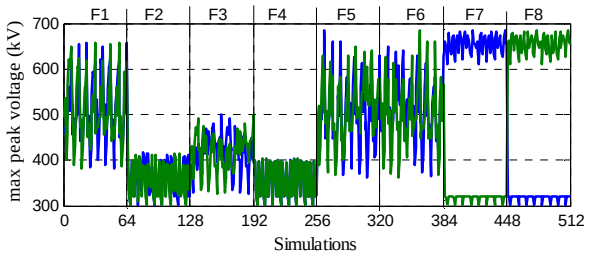


Figure 4: Maximum overvoltages on V_{dc}^{-} (blue) and V_{dc}^{+} (green)

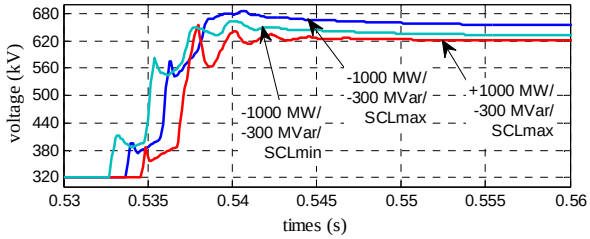


Figure 5: Time domain waveforms of V_{dc}^{+} due to F8

2) AC primary overvoltage

Figure 6 shows the maximum overvoltage registered for each simulation for the primary three phases $v_{prim_{abc}}$. The maximum value is equal to 532 kV. Typical configuration that leads to this overvoltage is F1 fault type. Nevertheless, for the simulated test cases, the maximum overvoltage on the primary AC side is lower than the overvoltage that can be generated from the AC network. The impact of the SCL strength is illustrated in the time domain waveforms (Figure 7). One can notice, that the maximum peak overvoltage occurs during the AC breaker opening instant (around 50ms after fault occurrences) and not during fault instant. The fault current is inductive and leads to a switching overvoltage when it is interrupted by BRK1.

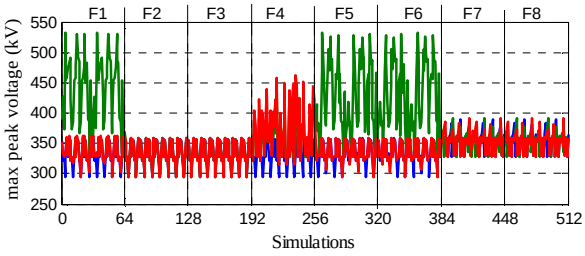


Figure 6: Overvoltage on AC primary side

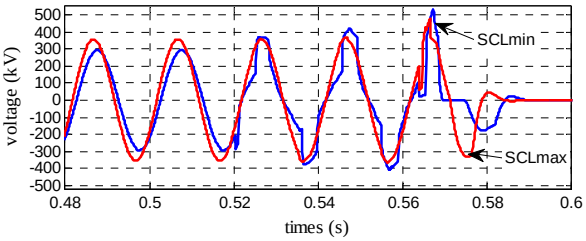


Figure 7: v_{prim_b} due to F1

3) AC secondary overvoltage

Figure 8 shows the maximum overvoltage on $v_{\sec_{abc}}$ of each configuration. The phase-to-ground fault (F1) seems to be the fault type which generates the highest overvoltage on $v_{\sec_{abc}}$ around 675 kV. A strong SCL and with a capacitive reactive power transit tend to increase the overvoltage value. Note that fault types F5 to F8 generate also high overvoltage close to thus found during F1. The impact of the SCL on the AC secondary voltage phace C waveforms is depicted in Figure 9.

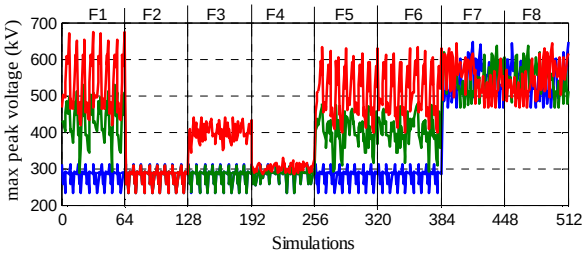


Figure 8: Maximum overvoltage on $v_{\sec_{abc}}$

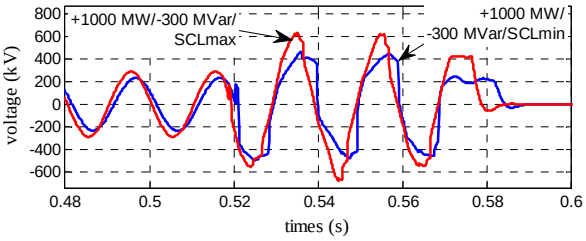


Figure 9: $v_{\sec_c}$ due to F1

4) Arm-to-ground overvoltage

The maximum overvoltage results of $v_{u\ell_{abc}}^{g}$ (i.e. six arm-to-ground measurements) are provided in Figure 10. The maximum peak reaches 814 kV during F1 fault. Strong SCL and with an inductive reactive power transit tends to increase the overvoltage value as depicted in Figure 11.

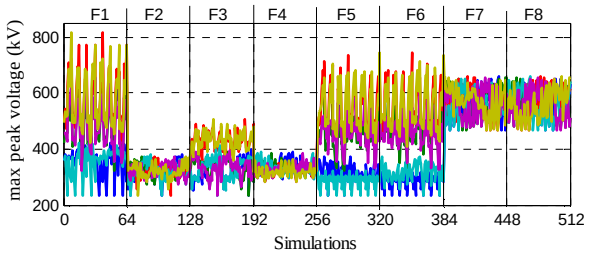


Figure 10: Maximum overvoltages on $v^{g}_{u\ell_{abc}}$

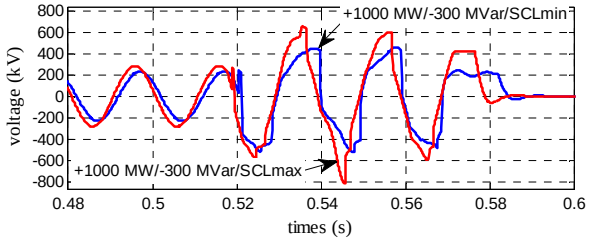


Figure 11: $v^{g}_{\ell_c}$ waveforms due to F1

5) Arm pole-to-pole overvoltage

The maximum overvoltage results of $v_{u\ell_{abc}}$ (i.e. six arm pole-to-pole measurements) are provided in Figure 12. The maximum peak reaches 1036 kV during F5/F6 and F1 fault. In this test case, strong SCL and with a positive active power transit tends to increase the overvoltage value as depicted in Figure 13.

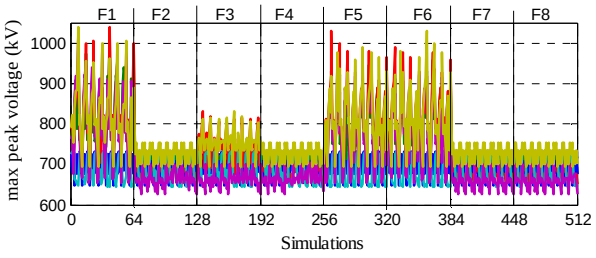


Figure 12: Maximum overvoltages on $v_{u\ell_{abc}}$

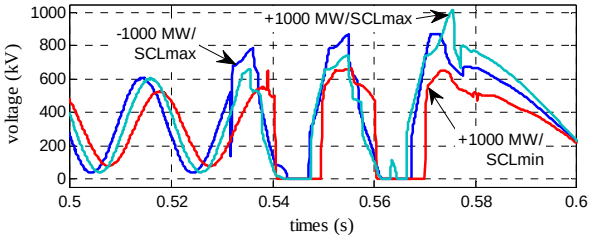


Figure 13: v_{ℓ_c} waveforms due to F1

B. Impact of arm inductance location

Converter station can have different circuit configuration depending on manufacturers and/or project specifications. In this section, the impact of arm inductance location is evaluated. The arm inductance that is located on the ac side terminal in Figure 3 is now placed on the dc side terminal of each arm. Faults F5 and F6 are kept between the valves and arm inductance. Same parametric studies, as depicted in Table 1, are simulated. Maximum overvoltage measurements of the DC pole-to-ground, AC secondary and arm pole-to-pole voltages are plotted in Figure 14, Figure 15 and Figure 16 respectively.

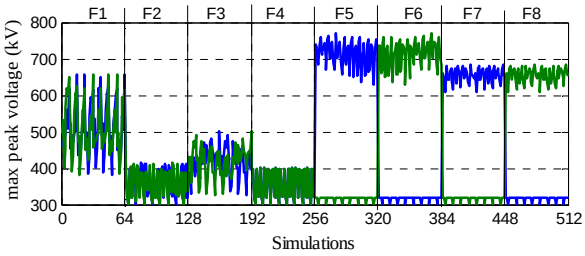


Figure 14: V^{-}_{dc} V^{+}_{dc} overvoltage - Arm reactor at DC side

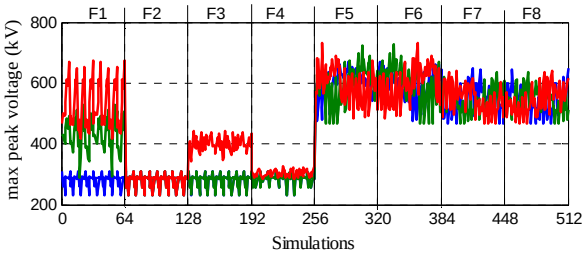


Figure 15: $v_{\sec_{abc}}$ overvoltage - Arm reactor at DC side

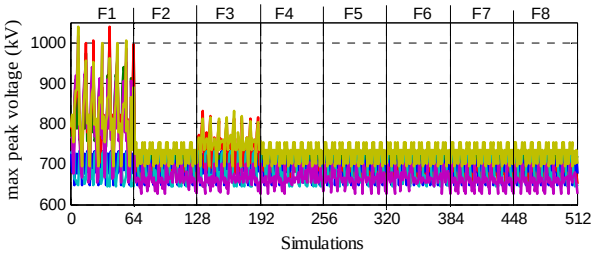


Figure 16: $v_{u\ell_{abc}}$ overvoltage - Arm reactor at DC side

Based on these results, it can be noticed that the arm reactor location has an impact on the overvoltage values and also on the fault type that lead to the worst case scenario. For V^{-}_{dc} and V^{+}_{dc} overvoltages, comparison between Figure 4 and Figure 14 reveals that when the inductance arm is placed on the dc side (instead of the ac side), the worst case are related with F5/F6 (rather than F7/F8). In addition, the maximum peak overvoltage is increased and reaches around 770 kV. For the ac secondary overvoltages (Figure 15), the F5/F6 fault type becomes the worst case (instead of the F1 fault type seen in Figure 8). Also the maximum peak overvoltage equal to 730 kV is increase when arm reactor is installed on the DC side. For $v_{u\ell_{abc}}$ overvoltages, arm reactor location does not have an impact on the maximum overvoltage value (1037 kV) and, as can be expected, when arm reactor is on dc side, only F1 faults lead to such high overvoltage.

C. Fault transient analyses

In this section the general behavior of the worst fault cases is analyzed. Based on previous results (section II.A.), it is noticed that the most critical faults are the F1 and F5 to F8. The general behavior of the DC pole-to-ground faults (i.e. F7

and F8) is reported in [5] and will not be further explained due to space limit. Moreover, the F5 and F6 faults are symmetrical, therefore only F5 is investigated because the behavior is identical.

In this section, the setup configuration of the link is -1000 MW/-300 MVar/ SCLmax and fault instant occurs at the maximum negative peak of v_{sec_a} (see Figure 17).

1) Phase-to-ground fault (F1)

For the considered configuration, F1 fault instant occurs at 0.532 sec. Overcurrent protection blocks the converter 600 µs after the fault instant and the AC breaker open at around 0.58 sec. As shown in Figure 17, a solid ground fault on phase A at the secondary side of the wye-delta transformer creates an overvoltage on phase B and C because the delta side reference to the ground has a high impedance. During fault instant, the faulty phase voltage is zero, therefore, v_{sec_b} and v_{sec_c} become equal to the phase to phase voltage of delta winding side (until the AC breaker opens).

The DC voltages and arm voltages of phase A are depicted in Figure 18 and Figure 19 respectivly. Before converter blocking, the voltage raise is limited by the arm inductor. It limits the inrush current coming from the SMs capacitors. Once the converter blocks, since the healthy phase to ground voltages become higher than the DC voltage, the lower freewheeling diodes of the each SM conduct (on the positive arm, when v_{sec_b} and v_{sec_c} are higher than V_{dc}^{+}, and vice versa). Therefore, V_{dc}^{+} and V_{dc}^{-} becomes almost equal to the maximum and minimum value of v_{sec_b} and v_{sec_c}. Hence the positive and negative DC voltages oscillate at the frequency of the AC system.

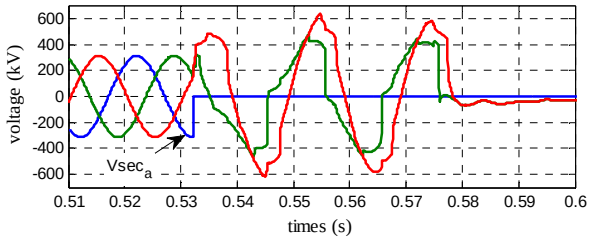


Figure 17: $v_{\text{sec}_{abc}}$ during F1

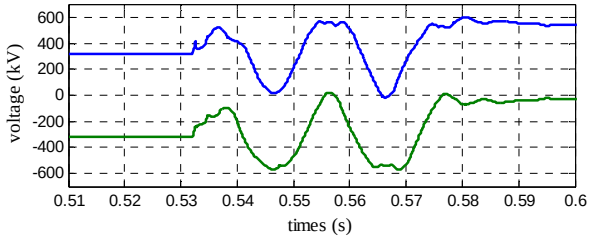


Figure 18: V_{dc}^{+} (blue) and V_{dc}^{-} (green) during F1

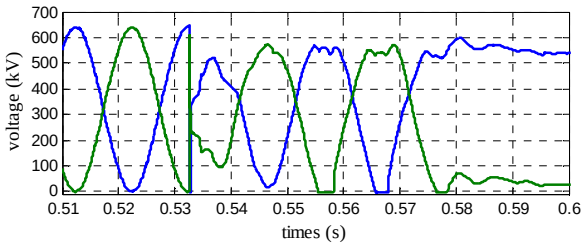


Figure 19: v_{u_a} (blue) and v_{ℓ_a} (green) during F1

2) Positive arm-to-ground fault (F5)

Converter behavior due to F5 is close to F1 since both faults are rather electrically similar (Figure 2).

Similar to previous case, the v_{sec_b} and v_{sec_c} following the fault, significantly increase as shown in Figure 20, but not as much as previous since the fault is not directly on the secondary winding side.

Overvoltages on DC voltages and arm voltages are depicted in Figure 21 and Figure 22 respectivly. Different behavior is noted between F1 and F5 faults during the time between the fault and blocking instant (around t=0.532 s). An equivalent circuit and a zoomed waveform, during this period intereval, is presented in Figure 23, Figure 24 and Figure 25. A voltage spike of around 640 kV is observed on V_{dc}^{+}. This overvoltage corresponds to the prefault arm voltage of v_{u_a} equal to 640kV (Figure 25) where one pole is abrutly clamped to zero when fault occurs. Unlike, internal bus fault in this case there is no arm inductance between the fault and the arms (except the IGBTs and diodes stray inductor) to limit the current raise. The current spike magnitude depends on the submodule capacitor values, the power electonic devices parasitic elements and the DC cable characteristics, therefore its value rely on the data accuracy. Nevertheless, switching overvoltage values of this phenomenon will not change drasticaly.

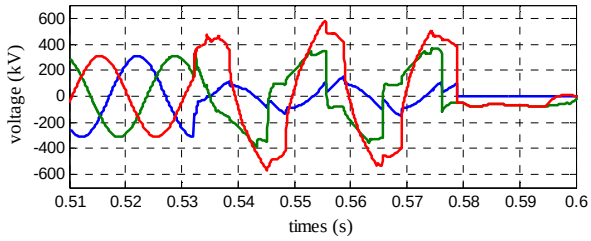


Figure 20: $v_{\text{sec}_{abc}}$ during F5

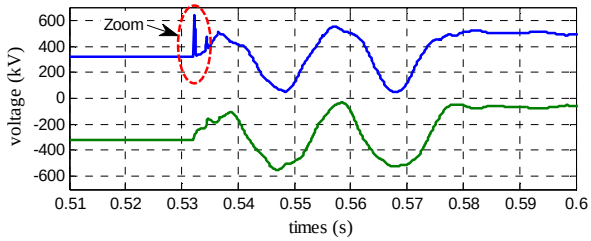


Figure 21: V_{dc}^{+} (blue) and V_{dc}^{-} (green) during F5

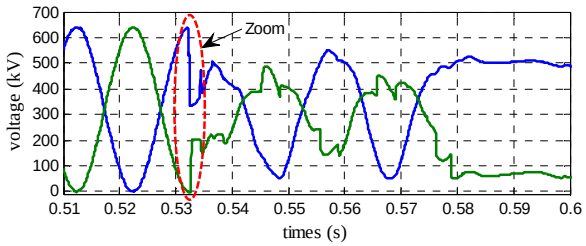


Figure 22: v_{u_a} (blue) and v_{ℓ_a} (green) during F5

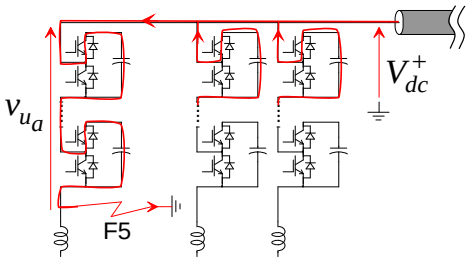


Figure 23: Equivalent circuit between fault and blocking instant (around t=0.532 s) of F5 fault

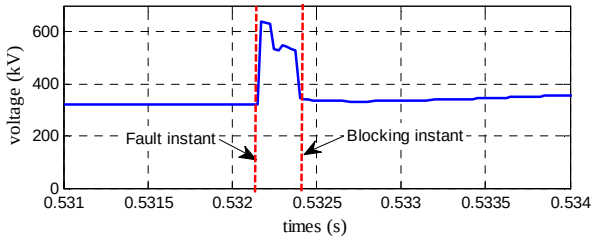


Figure 24: Zoom on V_{dc}^{+} during F5

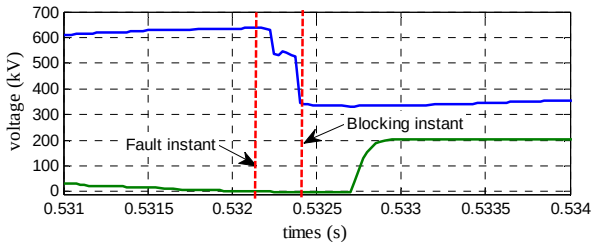


Figure 25: Zoom on v_{u_a} (blue) and v_{ℓ_a} (green) during F5

V. Influence of DC Surge Arresters

Based on the maximum switching overvoltage at the AC primary, AC secondary and arm to ground nodes, the Switching Impulse Protective Level (SIPL) can be selected accordingly to meet the insulation withstand level requirement.

However, transient overvoltages at DC poles (Figure 5) do not meet XLPE DC cable requirements. This overvoltage is composed of switching and temporary overvoltages that does not respect insulation coordination of the DC cable and can damage the XLPE insulation and cable junctions [5]. Several solutions exist to limit such overvoltage. A simple solution consists in the installation of several surge arresters at DC terminals. They must have a high energy rating since they are not only designed to limit switching overvoltages but also temporary overvoltages [5]. Based on the type test recommended in [11], a typical value that cable can withstand is in the range of 1.8 pu. In this paper, the characteristics of DC pole-to-ground surge arresters was chosen to meet this requirement.

Similar to previous sections, the same parametric study setup (section III.) has been simulated including the surge arresters, the MMC circuit and faults in Figure 2. The results of V_{dc}^{-} and V_{dc}^{+} including the surge arresters are presented in Figure 26. The total energy absorption of the surge arresters installed at the DC terminal are presented in Figure 27.

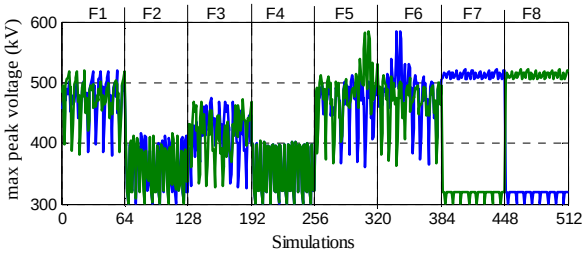


Figure 26: V_{dc}^{-} (blue) and V_{dc}^{+} (green) overvoltage including surge arresters

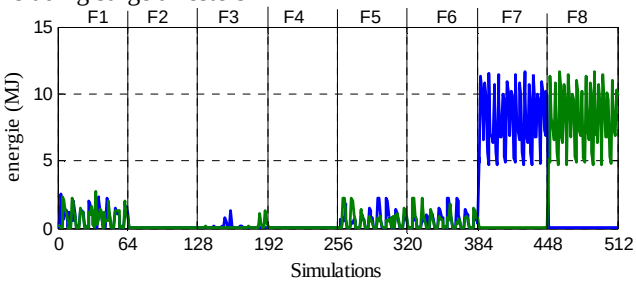


Figure 27: Energy absorptions of DC surge arresters

From Figure 26, we can notice that the maximum residual voltage is related to F5/F6 faults. As described in the subsection IV. C. , this overvoltage depicted during F5/F6 faults are expectable (when the arm inductance is at ac side - Figure 2) and are short (tens to hundreds of us) with high current value. Unlike F7/F8, the residual overvoltage induced by F5/F6 are only limited at 584 kV by the surge arresters since the inrush current produced from the capacitor's arm is high. Nevertheless, in case of F5/F6 faults, the energy absorbed by the DC pole-to-ground surge arresters is rather low (around 2 MJ) with respect to F7/F8 faults which reaches 12 MJ.

Time domain results of V_{dc}^{+} due to F8 faults are illustrated in Figure 28. The maximum peaks are now limited to 522 kV. These overvoltage values will change according to the design and characteristics of the surge arresters.

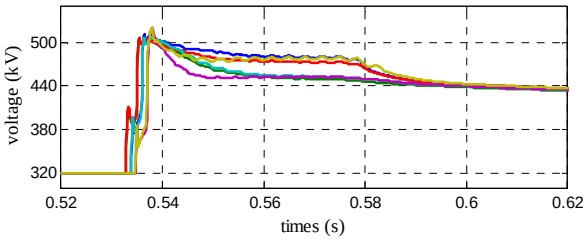


Figure 28: V_{dc}^{+} including surge arresters due to F8

VI. Conclusions

This article has presented a methodology to study transient overvoltages for HVDC-MMC link. A parametric studies (with 512 simulated configurations) using a generic HVDC-MMC link has been used. Transient overvoltage results due to several internal faults have been presented. It can be concluded that the main internal faults that lead to the highest overvoltages are the DC pole-to-ground, one phase-to-ground and arm-to-ground faults. Short-circuit level, active/reactive power transit have an impact on these overvoltage values.

The impact of the arm inductance location has been also investigated. The worst case scenario and overvoltage value are affected by the arm reactor location.

Finally, the inclusion and impact of the surge arrester design at DC terminal has been presented. It has been shown that for this specific example the higher residual voltage at dc terminal is related to F5/F6 faults (instead of F7/F8 faults). However, the highest energy absorption are related to F7/F8 faults.

VII. References

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