Effect of De-tuned Filter Energization on Supply Voltage Quality for VSDs

P. Marini

***Abstract*--In the latest years in most polypropylene petrochemical plants the requirements for power factor improvement, at the point of common coupling, has become more and more demanding by final plant users.**

In case of the energization of a capacitor bank, the main distribution voltage profile of the plant is subject to both transient voltage sags and voltage swells, and both types of voltage transients could affect the normal operation of variable speed drive (VSD) equipment fed by the same switchgear to which the capacitors are connected.

In this paper, a typical electrical distribution from an industrial plant is taken into consideration and the phenomenon of capacitor energization is studied by means of EMTP-ATP program: capacitors, which are equipped with series reactors to realize a de-tuned filter, are modeled on the basis of design parameters given by the relevant manufacturer.

Useful considerations and criteria, based on IEC standards for the electromagnetic compatibility, are carried out in order to specify a voltage withstand requirement which the VSD equipment connected to the distribution switchgear shall comply with, during the voltage transient caused by the energization of capacitors.

***Keywords*: capacitor bank, energization, de-tuned filter, power quality, variable speed drives (VSDs), electromagnetic compatibility.**

I. INTRODUCTION

THE requirement of power factor compensation in petrochemical as well as in most industrial plants, has become more and more frequent [3], [4], and usually the target power factor value at the point of common coupling for the plant user ranges from 0.92 lagging to 0.98 lagging.

Moreover, there is also the concomitant necessity of guaranteeing that the voltage total harmonic distortion does not exceed the contractual limits imposed by the distribution operators: as a consequence, large capacitor banks, equipped with de-tuned type series reactors [5], are needed for the aim of both compensating the overall power factor of the plant as well as for filtering the harmonic current distortion caused by the variable speed drives fed by the same switchgear to which the capacitors are connected. The series reactor is needed also to realize the function of inrush current limiter during the capacitor energization [3].

It is well known in technical literature that the energization of a capacitor generates a sort of short circuit event [1], [2]: the relevant inrush current gives rise to both sudden voltage sags and subsequent voltage swells in the supply network. This voltage transient can be easily detrimental for the correct operation of variable speed drive equipment if the rated power of the capacitor bank is large compared to the short circuit power available at the point of common coupling of the capacitor [8], [9]: in this paper a new criterion is defined for the electromagnetic compatibility of variable speed drives in order to sustain such voltage surges, as well as to check the suitability of the largest capacitor bank size to be used.

II. SYSTEM DATA AND MODELING

A. System Data

The electrical distribution scheme of a typical industrial plant, in which a large capacitor bank (5 MVAR rated size at 11 kV) is applied, is shown in Fig. 1. The capacitor is necessary both to compensate the power factor value (0.8 lagging) of the plant loads, and for filtering the harmonic currents injected by the largest VSD into the supply network.

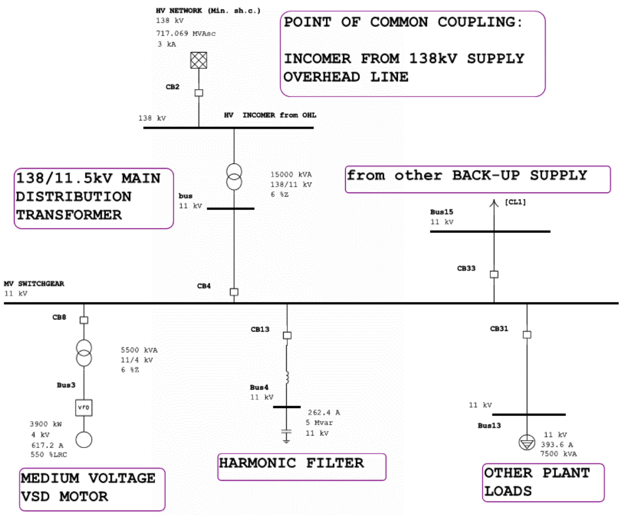

Fig. 1. Single-line diagram of the industrial electrical system

Main electrical parameters, for the main network components, are reported in the Appendix.

B. Modeling

For the aim of numerical simulation by ATP (Alternative Transient Program) [11], the electrical network is simplified and modeled as shown in Fig. 2, following the general guidelines presented in [10].

All equivalent impedances of the network components are

Paolo Marini is with the Department of Electrical Engineering, Maire Tecnimont Group, Milan, Italy (e-mail: p.marini@tecnimont.it).

Paper submitted to the International Conference on Power Systems Transients (IPST2019) in Perpignan, France June 17-20, 2019

referred to the capacitor bank rated voltage.

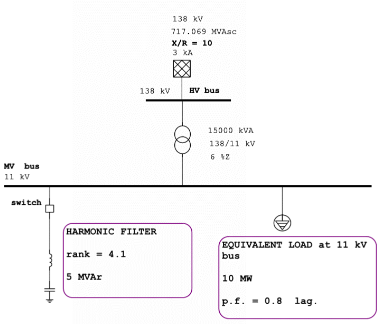

Fig. 2. Model of the tested electrical system

Main transformer is modeled by means of its short circuit impedance, while cables impedance can be neglected with respect to the one of transformer since they have very short length (few hundred meters at 11 kV). The equivalent impedance of the supply network is derived from the corresponding value of available minimum short power at the point of common coupling of the industrial plant to the supply grid.

The equivalent load is modeled as a constant R-L impedance: the variable speed drives are not modeled in detail since the main attention is put here on the transient voltage waveform originated by switching the capacitor on the minimum short circuit power of the supply network: the calculated prospective transient voltage is then compared with the voltage withstand values given by the VSD's manufacturer.

The capacitor is modeled as a series connection between the harmonic current blocking reactor (R-L component) and the capacitor (C component) for the power factor improvement, that is as a first order filter made of an R-L-C series connection. No additional damping resistor is connected in parallel to the capacitor and the reactor is air-core type.

The circuit breaker of the capacitor feeder is modeled as a time controlled switch, i.e. a switch that closes at a pre-determined time.

III. PRE-ANALYSIS AND ASSUMPTIONS

Before performing numerical simulations, few theoretical assumptions are first discussed to arrive at a useful criterion to judge the effects caused by the transient energization of the capacitor bank on the supply voltage.

A. *Phenomenon of capacitor energization*

It is well known from technical literature [6], that capacitor bank energization typically results in a low frequency oscillatory voltage transient with a primary frequency between 300 Hz and 900 Hz; this transient has a peak magnitude that can approach 2.0 p.u. , but is typically 1.3 p.u. to 1.5 p.u. , with durations between 0.5 cycles and 3 cycles of the fundamental, depending on the system damping.

Being the switching of a capacitor bank a common cause of transient overvoltage [12], in past years most attention and concern was put especially on the detrimental effect that this transient overvoltage could cause on the d.c. bus of voltage source inverter with consequent mal-operation an trip of the inverter [7], [8], [9]. But, in reality, it has to be pointed out that switching capacitor banks can cause also severe voltage sags which can as well affect the correct operation of variable frequency drive, since the voltage dip can make the drive to lose the torque control of the motor, both for VSDs based on load commutated inverter (LCI) technology and VSDs based on voltage source inverter (VSI) technology [16].

B. *Measuring of voltage sag and voltage swell*

Voltage sags and voltage swells are defined in several standards related to power quality [6], [12], [15]: here, the definition get from IEEE standard [6] is used:

- a sag (or dip) is a decrease in RMS voltage to between 0.1 p.u. and 0.9 p.u. for durations from 0.5 cycles to 1 minute.

- a swell is an increase in RMS voltage above 1.1 p.u. for durations from 0.5 cycles to 1 minute.

According to definitions of IEC standards for the electromagnetic compatibility [13], [14], voltage sags and voltage swells, related to low frequency transients such as capacitor energization events, can be monitored by measuring the R.M.S. voltage values taken over a minimum of one half of the period of the voltage at the supply frequency and refreshed each half-cycle (10 ms for 50 Hz and 8.33 ms for 60 Hz).

The main advantage of using a half-cycle window, compared to a one-cycle window, is a faster transition from the pre-fault voltage to the during-fault voltage and from the during-fault voltage to the post-fault voltage [13].

The half-cycle R.M.S. voltage calculated every sample is obtained by the following equation:

$$U_{RMS\,{}^1\!/_2}(n)=\sqrt{\frac{1}{N}\sum_{k=n-N+1}^{n}u(k)^2} \qquad (1)$$

where:

$U_{RMS\,½}$ = half-cycle R.M.S. value
n = generic sample discrete instant
N = number of samples per half-cycle
u (k) = sampled voltage waveform
k = 1, 2, 3, etc.

The half-cycle R.M.S. measuring is implemented in ATP by means of the feature TACS (transient analysis of control systems), as shown in the scheme of Fig. 3:

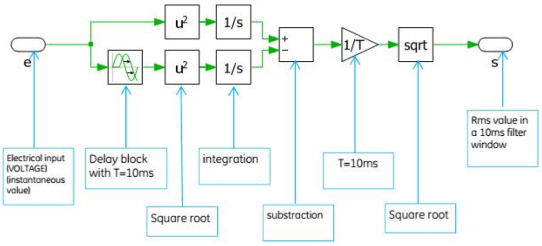

Fig. 3. Sliding window half-cycle RMS value calculation

C. *Definition of a voltage withstand requirement*

The main 11 kV variable speed drive in the system is based on LCI (Load Commutated Inverter) thyristor technology.

Upon agreement with VSD's manufacturer, the following voltage withstand requirements are used as design reference information to judge the effect of capacitor energization on the quality of the supply voltage to VSD:

R.M.S. value, measured with 10 ms sliding window, $U_{RMS\,½}$ shall be:

$U_{RMS\,½} \geq 85\%$ rated voltage, during a dip;
$U_{RMS\,½} \leq 115\%$ rated voltage, during a swell.

Moreover, VSD's manufacturer confirmed also that, in terms of instantaneous values being expressed in per unit of √2 times the single-phase to neutral supply voltage, the VSD can accept even an interruption of 0 p.u. for a maximum time duration of 10 ms, and it can accept an overshoot of 1.2 p.u. for a maximum time duration of 10 ms.

IV. RESULTS

The results of numerical simulations are shown graphically in the following figures. Inrush currents during capacitor energization, and bus bar voltages (both instantaneous values and half-cycle sliding window R.M.S. values), are chosen as the most significant magnitudes in order to evaluate the impact of the capacitor energization on the 11 kV distribution system.

A. *Capacitor energization transient phenomenon*

Capacitor is switched-on at time instant t = 0.02 s. Instantaneous inrush current for the most representative phase (phase A) is shown in following figure.

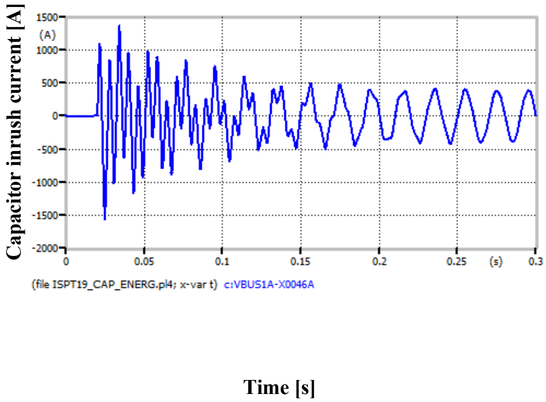

Fig. 4. Instantaneous capacitor inrush current (phase A) vs. time

As it can be seen, the transient energization takes practically almost 300 ms to be completed and it is clearly recognizable the typical low frequency current ripple superimposed on the 50 Hz fundamental current.

In the next figure, an enlarged view of the capacitor current is shown, to best highlight the maximum peak inrush current values and the oscillation period of the current ripple.

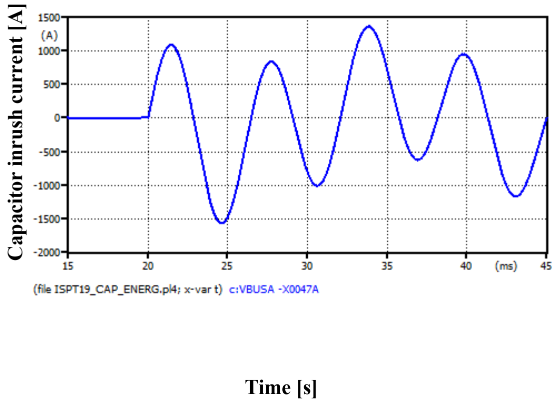

Fig. 5. Enlarged view of capacitor inrush current (phase A) vs. time

The first peak value of inrush current reaches approximately 1100 A on phase "A", while the oscillation period of the inrush current ripple has a frequency of about 159 Hz: these values are in good agreement with the results being manually calculated in the Appendix by applying the general formulae of technical literature [1].

B. *VSD's supply voltage at several switching instants*

The effect on voltage supply, in terms of voltage sags and voltage swells is then studied. The capacitor is switched-on at three different time instants, separated by 5 ms between each other:

$t_{1\_switching} = 0.02$ s, $t_{2\_switching} = 0.025$ s, $t_{3\_switching} = 0.03$ s .

In the next figure the instantaneous capacitor supply voltages are shown: the phase A is taken as reference for each event of energization.

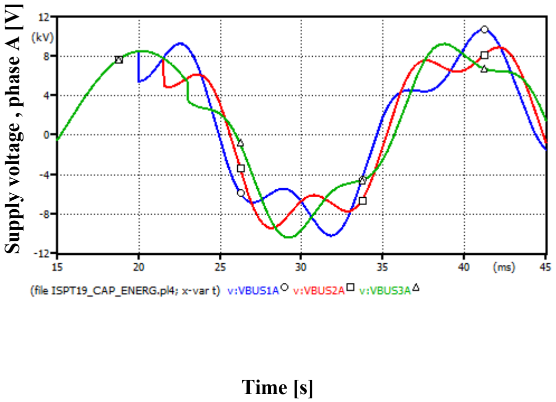

Fig. 6. Supply voltage as a function of time, at three switching instants

It can be seen that the sag caused by the energization on the network supply voltage is the same independently of the switching instant, while the voltage swell attains the highest value when the capacitor is switched-on at the instant of voltage peak.

The R.M.S. values are then evaluated by applying the half-cycle sliding window measurement to the above instantaneous values of the supply voltage.

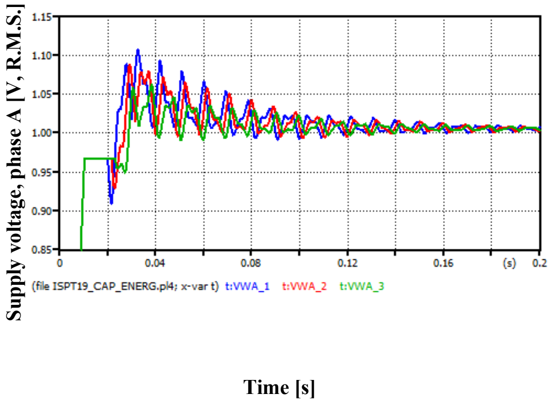

Fig. 7. Half-cycle R.M.S. supply voltage as a function of time

The worst half-cycle R.M.S. value, both in terms of voltage dip and voltage swell, is reached when the switching occurs at the instant of peak voltage.

In the next figure, an enlarged view of the VSD's supply voltage is shown, to best highlight the voltage dip and subsequent voltage swell.

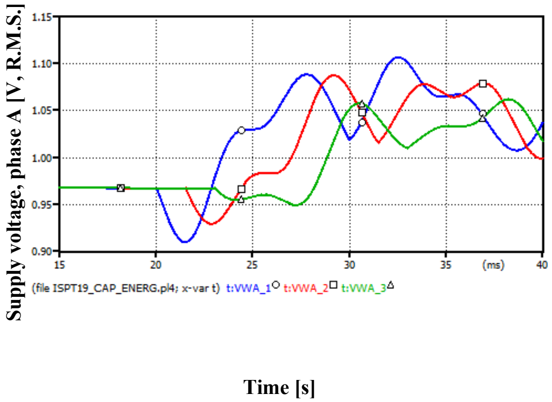

Fig. 8. Half-cycle R.M.S. supply voltage as a function of time (Zoom view)

It can be seen that the worst voltage dip attains almost 90% of rated voltage, while the worst voltage swell reaches almost 110% of rated voltage.

C. Simulations versus manufacturer information

No violation of the quality criterion for the VSD's supply voltage occurred:

- <u>Voltage dip on VSD's supply voltage (half-cycle R.M.S.):</u> calculated 0.90 p.u. versus reference 0.85 p.u.
- <u>Voltage swell on VSD's supply voltage (half-cycle R.M.S.):</u> calculated 1.10 p.u. versus reference 1.15 p.u.

D. Feedback from plant operation

The industrial plant has been operating for more than five years since its first commissioning and along this period the scheduled shutdown and subsequent restart were executed two times due to maintenance activities.

As per information get from plant operation personnel, no undue trip of VSD equipment ever occurred, neither during the normal operation nor during the first startup and subsequent restarts of the plant.

V. CONCLUSIONS

In this paper a typical industrial distribution system, which supplies a large capacitor bank (5 MVAR at 11 kV), is analyzed for the aim of studying the effect of capacitor energization on the voltage profile which supplies medium voltage variable speed drive equipment. This capacitor size can be defined large for the 11 kV voltage level, since the relevant rated current (262 A) is close to the maximum permissible size of the medium voltage switchgear's circuit breaker which can be commercially selected (400 A).

The energization of such capacitor is a normal switching event, due to the fact that the capacitor is switched-off each time that the plant works under very low load conditions (e.g. during pre-commissioning, maintenance, partial production of chemical product), and then switched-on as soon as the full load condition is reached again or the scheduled maintenance condition in some portion of the plant is cleared. In industrial plants with such not so high voltage levels (11 kV), it is neither common practice nor commercially affordable to use controlled switching techniques to energize the capacitors in order to suppress the voltage transient, as is well described in the technical literature [7].

Depending on the random switching instant of the capacitor power-on, the resulting transient voltage could be in principle also almost null for a brief time duration (e.g. 0.5 ms to 2 ms): hence, it is not significant to base on the instantaneous voltage values in order to assess the immunity of variable speed drive (VSD) equipment to such voltage surges, considering that the control logics of variable speed drives is mainly sensitive to the R.M.S. supply voltage value, as confirmed by drive manufacturers.

From the voltage dip point of view, the closing time of the circuit breaker which feeds the capacitor bank has no influence. From the voltage swell point of view, the maximum overvoltage appears for closing times corresponding to the maximum value of the phase voltage.

The variable speed drive can mal-operate both in case of voltage overshoots which make trip the inverter d.c. bus protections due to overvoltage [8], [9], and in case of voltage sags which make as well trip the drive due to loss of torque control of the motor, especially for VSDs which are based on load commutated thyristors converters [16].

A new simple electromagnetic compatibility criterion to assess the power quality of the voltage supply for the variable speed drive equipment was found, following the guidance given by drive manufacturers and based on the positive feedback about the healthy operation of drive equipment received by plant personnel during five consecutive years of plant operation:

- the R.M.S. value of the supply voltage shall be derived by using a measuring sliding window having 10 ms time frame and by refreshing the measuring each 10 ms, as per IEC Std. definition [12], [13];

- the R.M.S. value of the supply voltage shall be less than 115% of rated value;
- the R.M.S. value of the supply voltage shall be higher than 85% of rated voltage.
- if the R.M.S. value of the supply voltage during the transient capacitor energization does not comply with the previous two conditions, it is necessary to split the capacitor bank in sub-steps, each one having a lower rated power, and to perform again the energization study to check the correctness of the adopted solution.

The above criterion is especially useful at an early design stage of the electrical distribution of an industrial plant.

No detailed information was available from VSD manufacturer regarding the drive control logics: in future this work could be further improved by modeling in detail the VSD components and the relevant torque versus speed inverter control and voltage versus speed inverter control, in order to best assess how transient supply voltages can affect the VSD control.

VI. APPENDIX

A. *Electrical Network Components Data*

TABLE I
SUPPLY NETWORK

Equipment	Parameters
Equivalent Network at the point of common coupling for the industrial plant	138 kV rated voltage
	50 Hz rated frequency
	1195 MVA min. 3-phase short circuit power
	5 kA min. 3-phase sub-transient short circuit current at rated voltage
	X/R = 10 reactance to resistance ratio
	L_N = 0.3223 mH inductance/phase (at 11 kV)
	R_N = 0.0101 Ω resistance/phase (at 11 kV)

TABLE II
DISTRIBUTION TRANSFORMER

Equipment	Parameters
Transformer dedicated to the supply of main distribution 11kV switchgear bus bar	15 MVA rated power
	33 / 11.5 rated voltage ratio
	Z_T = 10% short circuit impedance (referred to rated power)
	L_T = 2.57 mH inductance/phase (at 11 kV)
	R_T = 0.0403 Ω resistance/phase (at 11 kV)

TABLE III
CAPACITOR BANK

Equipment	Parameters
Capacitor: - improves the power factor - single regulating step with manual control	11 kV Rated operating voltage
	5 MVAR Rated operating reactive power
	262 A Rated operating current
	C = 131.53 μF capacitance/phase
	X_C = 24.2 ohm Capacitor reactance/phase
	Double-Star phase connection
Series reactor: - limits the capacitor inrush current - filters the harmonic currents generated by VSD equipment	L_L = 4.62 mH Reactor inductance/phase
	R_L = 0.097 Ω Reactor resistance/phase
	X_L = 1.45 Ω Reactor reactance/phase
	$r = \sqrt{(X_C/X_L)} = 4.1$ harmonic tuning factor of the L-C filter
	Air-core reactor type

B. *Equations for capacitor energization transient*

Here after the main equations are reported in order to get in simplified way the main behavior of the energization transient, on the basis of well-known technical literature [1]:

$$Z_S = \sqrt{\frac{L}{C}} = \sqrt{\frac{(L_N + L_T + L_L)}{C}} = \quad 7.56 \quad \Omega \tag{2}$$

where:
Zs = surge impedance of the circuit
L = total inductance of the circuit
C = capacitance of the capacitor

$$\lambda = \frac{Z_S}{R} = \frac{Z_S}{(R_N + R_T + R_L)} = \quad 51.3 \tag{3}$$

where:
λ = damping factor of the circuit
Zs = surge impedance of the circuit
R = total resistance of the circuit
λ > ½ → the transient behavior of the circuit is damped oscillatory

$$\tau = 2 * \frac{L}{R} = \quad 102 \text{ ms} \tag{4}$$

where:
τ = damping time constant
L = total inductance of the circuit
R = total resistance of the circuit

$$T = \frac{2\pi}{\left(\sqrt{4\lambda^2 - 1}\right)/\tau} = \quad 6.25 \quad \text{ms} \tag{5}$$

where:
T = oscillation period
π = pi-grec number (approx. 3.14159)

λ = damping factor
τ = damping time constant

$$f = \frac{1}{T} = \quad 160 \quad \text{Hz} \tag{6}$$

where:
f = oscillation frequency
T = oscillation period

$$I_p = \sqrt{\frac{2}{3}} \cdot \frac{U_N}{Z_S} = \quad 1188 \quad \text{A} \tag{7}$$

where:
I_p = peak value of inrush current
U_N = operating system voltage (11000 V)
Z_S = surge impedance of the L-C oscillating circuit

C. Characteristic impedance of Harmonic Filter

The harmonic filter made of the series connection between capacitor bank and series reactor, has the following impedance versus frequency (frequency scan plot for phase A):

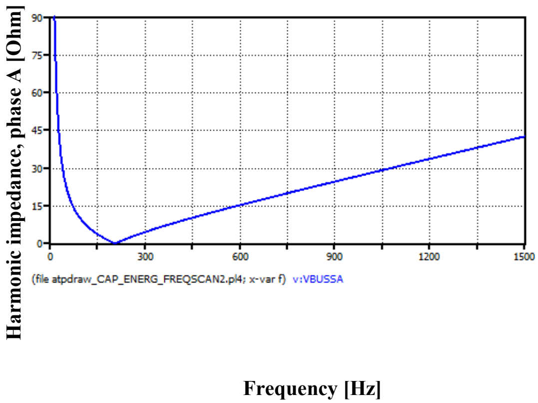

Fig. 9. Impedance of the capacitor-reactor filter as a function of frequency

It can be clearly seen the tuning frequency of the filter, equal to approximately 205 Hz (which is 4.1 times the fundamental value of 50 Hz), and for which the impedance becomes ideally null (neglecting the series resistance of reactor) due to the resonance condition between capacitor and series reactor.

VII. ACKNOWLEDGMENT

The author gratefully acknowledges the Electrical Department of Maire Tecnimont Group, for the consultation of the available technical literature.

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