A Reduced-Order Model of Full-Bridge Modular Multilevel Converter for the Analysis of Electromagnetic Transients

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***Abstract*—This paper presents a detailed equivalent model (DEM) of the full-bridge modular multilevel converter (FB-MMC) for analysis of electromagnetic transients in power systems. The proposed FB-MMC model of each MMC arm is based on (i) developing an equivalent model of each full-bridge sub-module (FB-SB) and (ii) combining all FB-SB models, in each simulation time-step. The salient feature of the model is that it also accounts for switching status of anti-parallel diodes of switch cells within each FB-SM. Thus, the model can accurately represent both normal and blocked modes of FB-MMC operation with the required accuracy for system-level studies. The proposed DEM is also advantageous for hardware-in-the-loop (HIL) CPU/FPGA-based real-time simulation of large power systems, e.g. HVDC grids. Performance of the proposed model, based on case studies of an FB-MMC HVDC test system, is presented and verified versus the results obtained from component-level model (CLM) representation of the FB-MMC in PSCAD environment.**

***Keywords*—Full-bridge modular multilevel converter, electromagnetic transients, DC-side faults, modeling.**

I. Introduction

THE modular multilevel converter (MMC) has been established as an economically and technically viable technology for HVDC system applications [1]–[3]. This necessitates the development of MMC models for various types of power system studies, including analysis of power system electromagnetic transients (EMTs), e.g., analysis and performance evaluation of protection system strategies and algorithms.

Due to the large number of sub-modules (SMs) in each arm of MMC, component-level model (CLM) of MMC in which all SMs and the associated components are individually represented, is not a computationally viable option for time-domain simulation of EMTs [4]. This has resulted in significant effort to develop MMC equivalent models which provide computational efficiency and required accuracy for time-domain simulation of EMTs. The model development effort has been mainly focused on the half-bridge (HB) MMC configuration [5]–[13] since the existing operational MMC-HVDC stations and the foreseeable future MMC installations use the HB-MMC configuration [14].

The full-bridge (FB) MMC configuration provides all technical features of the HB-MMC, and also enables DC-side fault-current blocking [15]–[18]. This feature is of significance in the protection of MMC-based HVDC grids [19]. The drawback of FB-MMC as compared with HB-MMC is the larger number of switch cells, i.e., two more switch cells per each SM. This drawback can be fully or partially justified in HVDC-grid applications where the DC-side fault-current blocking capability of FB-MMC can reduce sizes and maximum ratings of HVDC-grid current-limiting reactors and DC breakers. To evaluate the performance of FB-MMC for HVDC system applications in the context of EMTs, similar to the HB-MMC, there is a need for an equivalent model of the FB-MMC that can provide the desired computational efficiency and the required accuracy. The reported FB-MMC models for EMTs studies include:

- Accelerated model [10] - This approach reduces the size of the admittance matrix by treating each SM as a separate sub-system. Although the accelerated model accurately represents the FB-MMC under normal conditions, it cannot properly represent its behavior during blocked-mode scenarios, e.g., during DC-side faults [9].
- Thevenin equivalent model [13] - This approach represents the FB-MMC by a Thevenin voltage source and an equivalent series resistance in each simulation time-step and provides an accurate representation of FB-MMC during normal conditions. However, it is unable to represent the converter behavior during the blocked mode, as it does not take into account the blocked state of the switching elements [12].
- Continuous model [20] - This approach represents a detailed equivalent model of an MMC with either HB or FB configuration based on the continuous generic components available in most EMT software libraries. In this context, the model of [20] can properly represent the FB-MMC behavior under the blocked mode of operation. However, a model based on the discretized representation of the component equations is required for its digital implementation in CPU/FPGA for real-time simulation.

This paper proposes a detailed equivalent model (DEM) of the FB-MMC based on the Thevenin equivalent model approach [11], [12]. The proposed DEM accurately represents the behavior of the FB-MMC under both normal and blocked modes of the operation, including during DC-side faults. This is accomplished by taking into account the natural commutation process of the anti-parallel diodes. To validate and verify the performance of the proposed DEM, its dynamic behavior under various operating conditions in an FB-MMC-based HVDC system is investigated. The study results reveal that the proposed DEM results closely match those obtained

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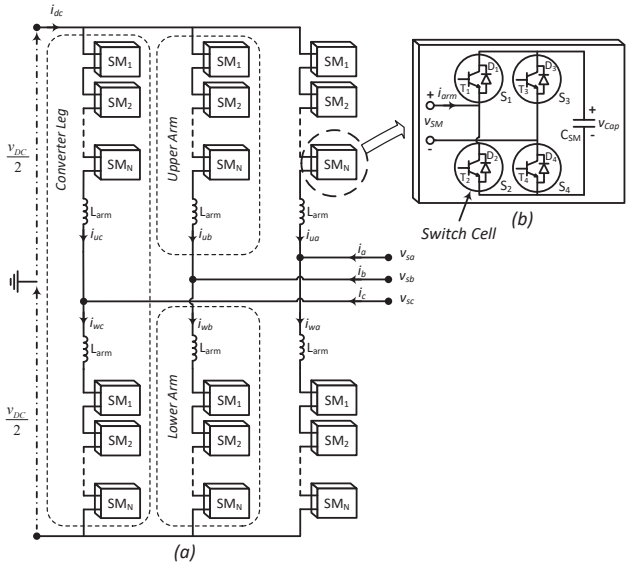


Fig. 1. A schematic diagram of: (a) FB-MMC, and (b) FB-SM.

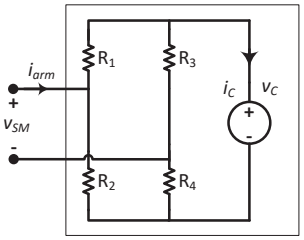
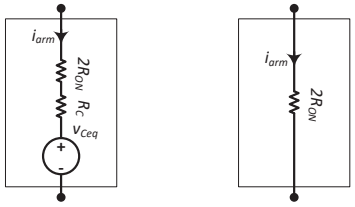


Fig. 2. Equivalent model of FB-SM.



(a) Inserted SM (b) Bypassed SM

Fig. 3. Thevenin equivalent models of FB-SM.

from its CLM counterpart.

II. Equivalent Model of FB-MMC

Fig. 1(a) shows a schematic diagram of a three-phase FB-MMC for which the arms have identical structures and each consists of N identical series connected FB-SMs and an arm inductor L_{arm}. Operational principles of FB-MMC are provided in [21] and [22]. FB-MMC has 1) normal operation mode, and 2) blocked operation mode. During the normal operation mode, each SM can be inserted (in service) or bypassed by its gating signals. The reverse polarity of FB-SM is not exploited in the normal operating conditions [19]. In the blocked mode, all the gating signals are disabled and the current conduction path is determined based on the natural commutation process and the arm current direction. FB-MMC is required to be blocked upon the detection of a DC-side pole-to-pole fault.

A. Normal Operation Mode

The proposed DEM of FB-MMC, under normal operation mode, is developed based on the modeling approach of [11] and [12]. Each MMC arm is modeled by a Thevenin equivalent circuit during each simulation time-step and used for numerical solution of the system equations. Due to the series connection of FB-SMs in each arm, in each simulation time-step, the arm Thevenin equivalent circuit is the series connection of the Thevenin equivalent circuits of all corresponding SMs, in series with the arm inductor L_{arm}. To obtain the Thevenin equivalent circuit of each SM, each switch cell is treated by a two-state resistance where the ON (OFF) switch is represented by a small (large) resistance. Meanwhile, each SM capacitor, in each simulation time-step, is represented by the discretized form of

$$i_C(t) = C\frac{dv_C(t)}{dt}, \tag{1}$$

based on trapezoidal integration method [23], i.e.,

$$v_C(t) = v_C(t-\Delta T) + \tfrac{\Delta T}{C_{SM}}\left(\tfrac{1}{2}i_C(t) + \tfrac{1}{2}i_C(t-\Delta T)\right), \tag{2}$$

where C_{SM} is the SM capacitance, v_C is the capacitor voltage, i_C is the capacitor current, and ΔT is the simulation time-step. Based on (2), the SM capacitor is represented by a voltage source v_{Ceq} in series with resistance R_C, i.e.,

$$v_C(t) = R_C i_C(t) + v_{Ceq}(t), \tag{3}$$

where

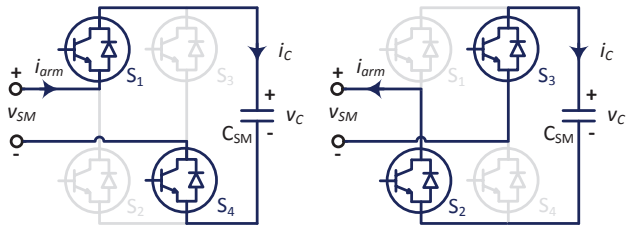
$$R_C = \frac{\Delta T}{2C_{SM}}, \tag{4}$$

and

$$v_{Ceq}(t) = 2R_C i_C(t-\Delta T) + v_{Ceq}(t-\Delta T). \tag{5}$$

In (3), v_{Ceq} represents the history term obtained from the SM capacitor current in the previous simulation time-step. Fig. 2 presents the equivalent circuit of the FB-SM configuration. Resistances R_1, R_2, R_3 and R_4 are determined based on the corresponding switching states and replaced by either on-state or off-state values at each simulation time-step. The calculation process of the SM Thevenin equivalent circuit can be further simplified, without losing the accuracy of the results, by treating each off-state switch as an open circuit [12]. Consequently, the SM Thevenin equivalent resistance is approximated by (i) the switch on-state resistances in series with R_C for inserted SMs and (ii) only switch on-state resistances for bypassed SMs. Meanwhile, the SM capacitor current magnitude and direction are the same as those of the arm current for inserted SMs and the current is zero for bypassed SMs.

For each inserted or bypassed SM, two switch cells are in the current path, and the SM capacitor representation appears



(a) Positive arm current (b) Negative arm current

Fig. 4. Possible current paths through the switch cells of the FB-SM under the blocked mode based on the arm current direction.

in the model only for the inserted SM. Therefore, the Thevenin equivalent model of each inserted SM is a voltage source v_{Ceq} in series with R_C and two R_{ON} resistances. Each bypassed SM can be represented only by two R_{ON} resistances as the SM capacitor is not in the current path. Fig. 3 shows the Thevenin equivalent models of the inserted and bypassed of each SM. The SM capacitor cannot be charged to a negative voltage due to the presence of anti-parallel diodes. To take this into account, the SM capacitor voltage is reset to zero for negative values. Under normal operation mode, the arm Thevenin equivalent voltage source v_{arm} and resistance R_{arm} are

$$v_{arm} = \sum_{i=1}^{N} v_{Th_{SM_i}}, \tag{6}$$

where

$$v_{Th_{SM_i}} = \begin{cases} v_{Ceq_i}, & \text{Inserted SM (Positive Polarity),} \\ 0, & \text{Bypassed SM,} \\ -v_{Ceq_i}, & \text{Inserted SM (Negative Polarity),} \end{cases} \tag{7}$$

and

$$R_{arm} = n \times R_C + 2 \times N \times R_{ON}, \tag{8}$$

where n is the number of inserted SMs in the arm at each simulation time-step and N is the total number of SMs in the arm.

B. Blocked Operation Mode

FB-MMC is in the blocked mode upon disabling gating signals for all SMs in which the arm current path determined based on the natural commutation process. Thus, conduction characteristics of anti-parallel diodes also have to be taken into account based on the arm current direction. Fig. 4 presents possible current paths through FB-SM switch cells under a blocked mode.

When the arm current is positive, it passes through S_1, S_4 and the SM capacitor, as shown in Fig. 4(a). Under this condition, the capacitor current has the same magnitude and direction as those of the arm current. When the arm current is negative, it passes through S_2, S_3 and the SM capacitor, as shown in Fig. 4(b). Under this condition, the capacitor current has the same magnitude but with the opposite direction as that of the arm current. The SM capacitor is charged for either positive or negative arm current directions. In addition, since all the series connected SMs in an arm are inserted in the current path under the blocked mode, the arm Thevenin

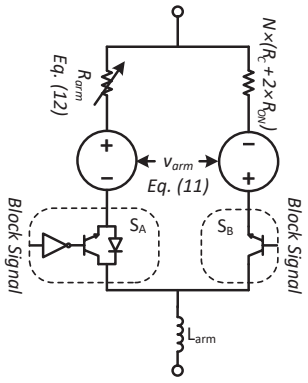


Fig. 5. Proposed FB-MMC arm equivalent model.

equivalent voltage source v_{arm} and resistance R_{arm}, obtained by (6) and (8), need to be modified as

$$v_{arm} = \sum_{i=1}^{N} v_{Ceq_i}, \tag{9}$$

$$R_{arm} = N \times (R_C + 2 \times R_{ON}). \tag{10}$$

In the blocked operation mode, the arm Thevenin equivalent voltage and resistance are the same for either positive or negative arm current directions.

C. FB-MMC Arm Equivalent Model

Fig. 5 presents circuit representation of the proposed arm equivalent model of FB-MMC. The blocked mode must represent the natural commutation process subsequent to the gate blocking. Therefore, ideal switches S_A and S_B of Fig. 5 are included in the model to take into account switching characteristics of SMs.

During a normal operation mode, as the block-signal is inactive, S_A is ON and provides bidirectional flow of the arm current while S_B is OFF and thus, the corresponding branch is open-circuit. The arm Thevenin equivalent voltage source v_{arm} and resistance R_{arm} are provided by (6) and (8), respectively.

During a blocked mode, the block signal is active and opens ideal IGBT S_A to represent the arm circuit for the positive arm current direction as shown in Fig. 4(a). Thus, S_B is ON to represent the arm circuit for the negative arm current direction as shown in Fig. 4(b). Therefore, the arm Thevenin equivalent voltage source v_{arm} and resistance R_{arm} are obtained based on (9) and (10), respectively.

Thus, the arm Thevenin equivalent voltage source v_{arm} and resistance R_{arm} of the FB-MMC arm equivalent model of Fig. 5 are obtained from

$$v_{arm} = \begin{cases} \sum_{i=1}^{N} v_{Th_{SM_i}}, & \text{Normal Operation Mode,} \\ \sum_{i=1}^{N} v_{Ceq_i}, & \text{Blocked Operation Mode,} \end{cases} \tag{11}$$

$$R_{arm} = \begin{cases} n \times R_C + 2 \times N \times R_{ON}, & \text{Normal Operation Mode,} \\ N \times (R_C + 2 \times R_{ON}), & \text{Blocked Operation Mode.} \end{cases} \tag{12}$$

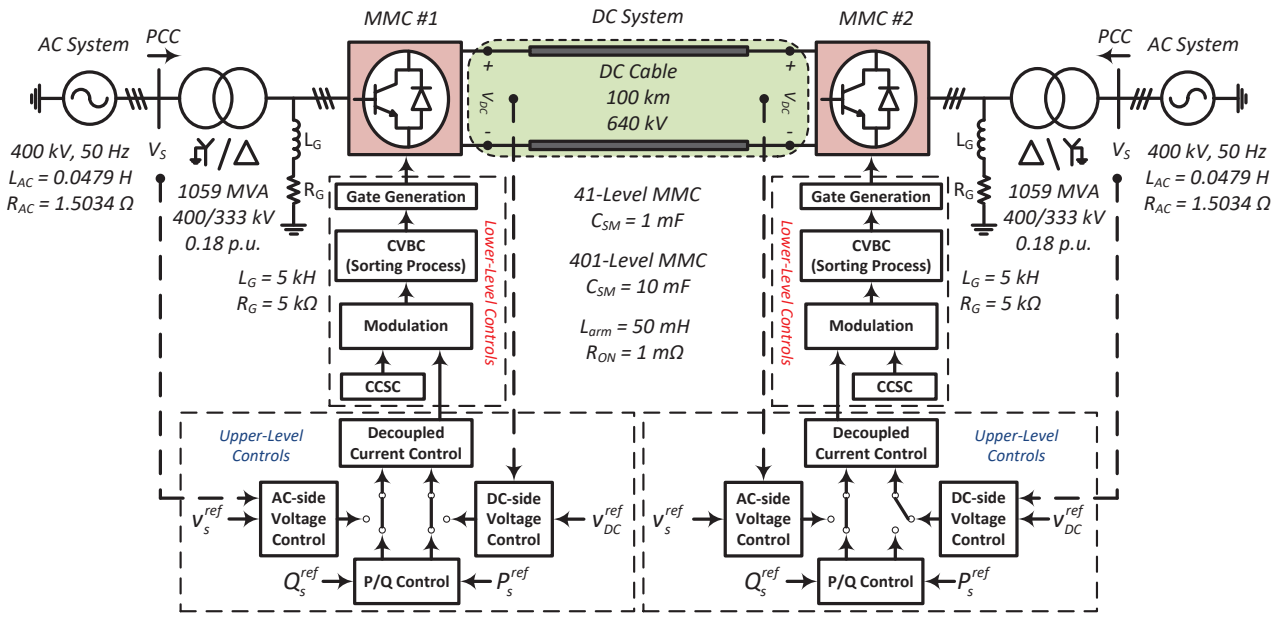


Fig. 6. A schematic diagram and parameters of the test system.

III. Test System

To evaluate performance and verify the accuracy of the proposed DEM, the test system of Fig. 6 is considered. The test system represents a monopolar, symmetric MMC-based HVDC link which interfaces two AC systems. The structure and parameters of the system are those of the HVDC link of [14], except that each HB-MMC of [14] is replaced by an FB-MMC of Fig. 1. The studies reported in this work are based on digital time-domain simulation in PSCAD/EMTDC platform using simulation time-step of 1 μs. Comparison of the corresponding results based on the proposed DEM and CLM is used for verification of the DEM. The component modules for the PSCAD-based simulation studies are as follows:

- Each MMC station is represented by a 41-level FB-MMC which is a reduced version of the actual 401-level FB-MMC, i.e., each 10 FB-SMs are represented by one equivalent FB-SM of 16 kV and SM capacitor of 1000 μF.
- Each AC system is represented by a three-phase AC voltage source with the short-circuit capacity of 10 GVA.
- The DC-link cables are represented by the frequency-dependent cable model [12].

Fig. 6 also shows the block diagram of the MMC control system. Each MMC control system has the upper- and lower-level hierarchy. The upper-level controller is based on the dq-frame vector control and generates the modulation signals corresponding to the converter set-points. The rotating dq-frame is aligned with phase-A voltage of the AC-grid. The lower-level controller generates the SM gating signals based on the modulation signals. The circulating current suppressing controller (CCSC) is also based on the dq-frame vector control and mitigates the circulating current by modifying the modulation signals [24]. The modulation stage determines the required number of SMs for insertion in each arm and is based on the phase-disposition PWM (PDPWM) method [25]. The capacitor voltage balancing control (CVBC) is based on the post-modulation balancing method [26]. The SM gating signals are reassigned based on the required number of SMs for insertion, sorting results, and the arm current direction [26].

IV. Simulation Results

A. Temporary DC-side Pole-to-Ground Fault

Fig. 7 presents the transient response of the study system of Fig. 6 to a temporary DC-side pole-to-ground fault. Initially, MMC-1 is under power-control and exchanges 800 MW and 200 $Mvar$ with the corresponding AC grid. MMC-2 regulates the DC-side voltage at 640 kV and operates at unity power factor. The fault occurs at the middle of the cable at $t = 0.4\ s$ with 1 Ω resistance for 10 ms. To quantitatively evaluate the performance of the proposed model, root-mean-square error (RMSE) values of DC-side terminal voltage and current are calculated and presented in Fig. 8. A comparison of the results from the proposed DEM and those from its CLM counterpart verifies the accuracy and applicability of the model for this type of studies.

B. Permanent DC-side Pole-to-Pole Fault for DC Cable

To evaluate the performance of the proposed DEM at the event of a DC-side fault, the test system is subjected to a permanent DC-side pole-to-pole fault. The pre-fault operating conditions of the system are identical to those of the previous case study. The fault occurs at $t = 0.4\ s$ at the middle of the DC cable with 10 $m\Omega$ resistance. The protection system detects the fault when any of the arm currents exceeds the pre-specified 3 kA threshold and disables all the gating signals.

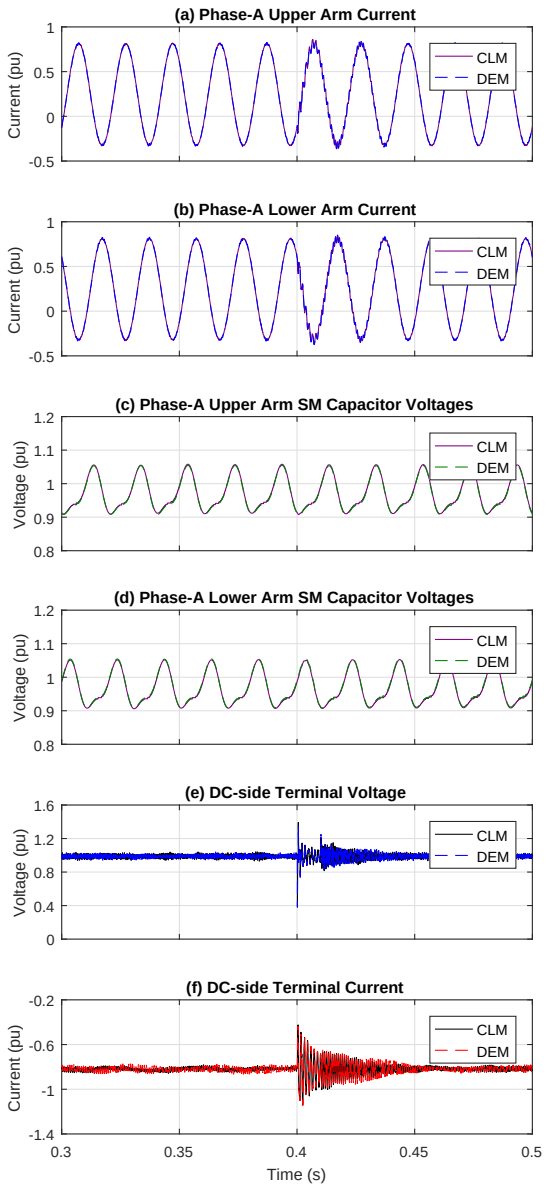


Fig. 7. Response of MMC-1 to a transient DC-side pole-to-ground fault scenario, obtained from the CLM and the proposed DEM.

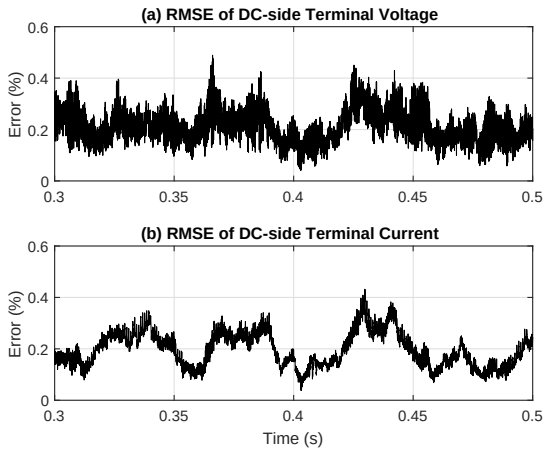


Fig. 8. RMSE values of DC-side terminal voltage and current for a transient DC-side pole-to-ground fault scenario.

Fig. 9 shows the dynamic behavior of the system, based on the CLM and the proposed DEM. Fig. 9(f) shows that the DC-side current starts to increase as the fault is applied. The protection system disables all the gating signals 550 μs after the fault occurrence as phase-C lower arm current reaches the protection limit. Upon disabling the gating signals, the fault current passes through the anti-parallel diodes of series connected SMs and charges the SM capacitors. As the sum of the capacitor voltages, connected in series, in the fault path is greater than the line-to-line AC-side peak voltage, the anti-parallel diodes become reverse biased and the fault current approaches zero. Therefore, the current path between the AC-side and DC-side is interrupted and the fault current approaches to zero. Fig. 10 presents RMSE values of DC-side terminal voltage and current. Comparison of the corresponding results from the CLM and the proposed DEM indicates that the proposed DEM accurately represents the blocked mode, particularly the inherent DC-side fault blocking capability of FB-MMC.

V. Conclusions

This paper proposed a detailed equivalent model for EMT analysis of full-bridge (FB) MMC. In the proposed model, each FB-MMC arm is represented by a Thevenin equivalent circuit at each simulation time-step and maintains a record of all SM capacitor voltages. The salient feature of the proposed model is that it enables accurate representation of the blocked operation mode by adding ideal switches to the existing models. Moreover, the proposed DEM is suitable for real-time simulation of realistic FB-MMC HVDC systems. The dynamic behavior of the proposed model is compared with its component-level model under DC-side faults. Results of these comparisons confirm that the proposed model accurately represents the FB-MMC behavior during steady state and transients of the power system, particularly at the event of a DC-side pole-to-pole fault.

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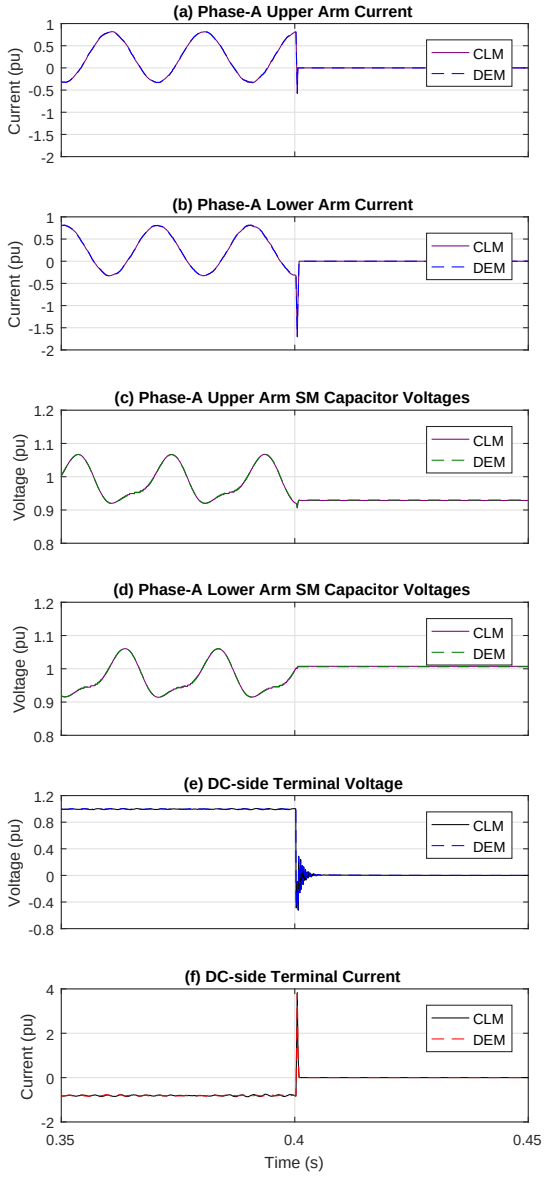

Fig. 9. Response of MMC-1 to a DC-side fault scenario, obtained from the CLM and the proposed DEM.

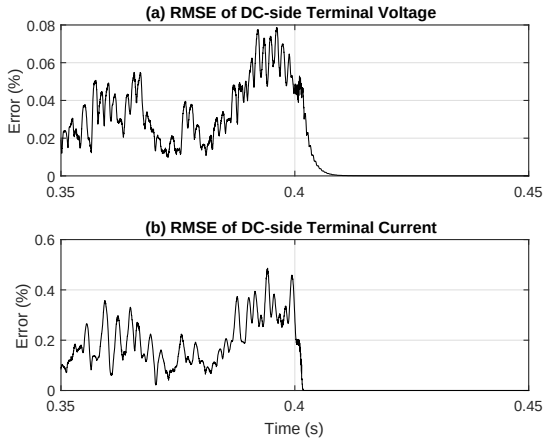

Fig. 10. RMSE values of DC-side terminal voltage and current for a DC-side fault scenario.

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