Zero-missing phenomenon after fault clearing

F. Faria da Silva, Claus L. Bak

***Abstract*— This paper analyses via simulations and theoretical demonstration, the possibility of zero-missing phenomenon after clearing a fault at a substation or its vicinity. The paper demonstrates how the phenomenon may occur and that the initial DC current of the shunt reactors may be larger than the shunt reactor peak AC current. As a result, zero-missing after fault clearing might be more severe than during the energisation of the cable in the same system. The impact of different system parameters is studied and the worst-case scenario defined. Typical countermeasures are ineffective for this case and a possible new countermeasure is introduced.**

***Keywords*: Zero-missing phenomenon, Shunt reactors, HVAC Cables, Reactive power compensation.**

I. Introduction

ZERO-MISSING phenomenon may occur when energising a shunt-reactor (SR) and a cable, or a long overhead-line (OHL), simultaneously if the magnitude of the transient DC current at the SR is larger than the sum of the AC current components of the SR and cable, which are virtually in phase opposition as the cable is unloaded. References [1]-[5] describe the phenomenon in detail and applicable countermeasures. The phenomenon is of concern, because of in case of asymmetric fault during zero-missing phenomenon, it may not be possible to open the sound phases in a safety manner until the current in those phases crosses 0A, which may take several seconds.

One common strategy to avoid zero-missing is to provide reactive power compensation via one or more SR at the substation and to energise the cable together with a SR that compensates less than 50% of the reactive power generated by the cable, avoiding both large voltage variations and zero-missing. Another strategy is to have all compensation connected directly at the busbar and to energise it separately from the cable.

If a fault occurs near a SR, the voltage at its terminals decreases to a low magnitude and the SR reenergises when the faults clear, at an uncontrollable time instant. As a result, the previous described countermeasures, which are efficient avoiding zero-missing phenomenon at energisation, have no impact for zero-missing after fault clearing, which depends on the fault location, fault impedance and network strength.

This paper analyses how zero-missing phenomenon may occur when a fault happens at a substation or in its vicinity. A theoretical explanation of the phenomenon is provided, by focusing on the magnitude of the DC current at the SR after clearing the fault. It is concluded that this DC current may be larger than the SR peak AC current and zero-missing more severe than for energisation. Furthermore, the countermeasures used for energisation are ineffective, except the installation of a permanent resistor. An alternative countermeasure is proposed, but it has some challenges, requiring further research.

II. Explanation of Zero-Missing Phenomenon After Fault Clearing in a Simplified System

The phenomenon is demonstrated first using the circuit from Fig. 1, consisting of two equal cables in series, with all reactive power compensation at the busbar. Cable A is compensated 50% at both ends, with Cable B compensated 60% at the left termination (SR_{B1}) and 40% at the right termination (SR_{B2}).

A three-phase-to-ground solid fault is simulated at the right end of CB_B. Fig. 2 shows the current measured at CB_{A1} and CB_{A2} after CB_B clears the fault. Zero-missing occurs in all three phases at CB_{A1} and in Phase A at CB_{A2}.

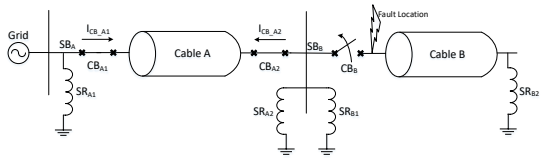

Fig. 1. Single-line diagram of simplified system for explaining the phenomenon

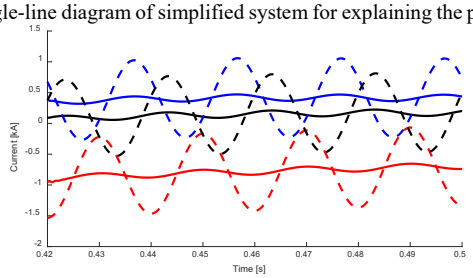

Fig. 2. Current in CBA1 (solid lines) and CBA2 (dashed lines). Phase A: red; Phase B: blue; Phase C: black

Focusing on phase A, Fig. 3 shows for Phase A, the current at both circuit breakers and at the two SRs close to the fault. Due to the 0V at the busbar during the solid fault, the current in the SR is a DC current during the fault, whose magnitude is the instantaneous current at the fault instant (peak AC current for this example). At the opening of the circuit breaker (CB), the voltage at the two SRs is restored, resulting in a decaying DC component at each SR (I_{SR_DC}), whose initial magnitude is the difference between the current in the SR immediately before fault clearing (I_{SR_FC}) and the instantaneous value of the SR's AC current component (I_{SR_AC}), as given by (1).

Equation (1) is rewritten as (2), where V_G is the peak voltage of the grid, X_{SR} is the reactance of the SR, θ_{FC} is the angle of the voltage at the instant the current in the CB extinguishes: i.e. $V_G\cos(\theta_{FC})$ is the voltage magnitude at that instant.

When the current in CB extinguishes, the voltage at the SR can be estimated using the voltage at the grid's reference point at the extinction instant; this approximation introduces an error

F. Faria da Silva and Claus L. Bak are with Aalborg University, Department of Energy Technology Denmark (e-mail of corresponding author: ffs@et.aau.dk)

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that can be corrected, as discussed next. The starting value of the AC current component (I_{SR_AC}) is approximately 90° phase displaced from the voltage and thus, the cosine in (2).

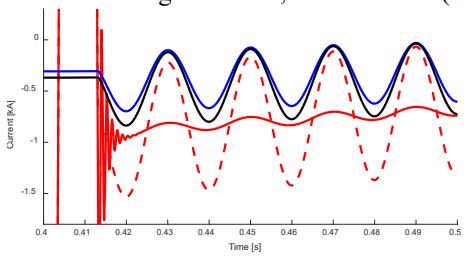

Fig. 3. Current in phase A at CB_{A1} (red solid), CB_{A2} (red dashed), SR_{A2} (blue) and SR_{B1} (black)

$$I_{SR\_DC} = I_{SR\_FC} - I_{SR\_AC} \tag{1}$$

$$I_{SR\_DC} = I_{SR\_FC} - \frac{V_{SR}}{X_{SR}} \Leftrightarrow I_{SR\_DC} = I_{SR\_FC} + \frac{V_G \cos(\theta_{FC})}{X_{SR}} \tag{2}$$

In the system of Fig. 1, the two SRs at SB_B compensate 110% of the reactive power generated by Cable A and as the fault occurs when the AC current of the SR is at peak value, the respective initial DC currents of the SRs at Phase A are larger than the AC peak currents, as explained next. In this context and as an example, the AC component of the current at CB_{A1} has a magnitude of approximately 10% the cable current, whereas the DC current magnitude is larger than 110% of the cable's current, resulting in zero-missing. A similar procedure happens for the other phases, but because the instantaneous current in those phases was smaller at the fault instant (I_{SR_FC}), the DC current has lower magnitudes.

III. Estimation of Initial DC Current in Shunt Reactors

The estimation of the angle θ_{FC} is critical for assessing zero-missing at fault clearance. θ_{FC} is the angle of the voltage at the instant the current at the CB extinguishes, but such is a source of error, as the voltage at a SR does not change instantaneously from 0V to the magnitude of the grid (V_G). The angle should be corrected to account for this transient, as shown in (3). For the system of Fig. 1, a radial connection exist and the reference point is at a defined distance, with a wave propagating at coaxial speed (180m/μs is a typical value) requiring τ_C seconds to go from one to the other. As a result, the correction of the angle for this case is given by (4) (where T is the period), which represents the angle at the instant corresponding to the wave propagating from the S_B to S_A and back to S_B. The angle can also be corrected using the series impedances, as demonstrated in (5)-(7), an easier method for more complex layouts.

$$I_{SR\_DC} = I_{SR\_FC} + \frac{V_G \cos(\theta_{FC} + \theta_l)}{X_{SR}} \tag{3}$$

$$\theta_l = 2\tau_C \frac{2\pi}{T} \tag{4}$$

Table I shows the initial DC current in SR_{B1} for the simulation of a single-phase-to-ground fault and two different clearing times, 40ms and 105ms. The fault initiates when the current at the SRs is at peak value for the faulted phase, remaining so during the fault. A decaying DC component at CB_B is still present when clearing the fault at 40ms, but mostly damped when clearing the fault at 105ms. Another important difference is that the point of wave of V_G for the faulted phase at the extinction instant is approximately 45° and 233° for 40ms and 105ms clearing times, respectively. These two clearing times were chosen in order to show two different aspects:

- Fault extinction with the DC fault current still present (40ms) versus a completely damped DC fault current (105ms);
- Opposite voltage polarities at the extinction instant, which impacts the magnitude of the initial DC current;

The shorter extinction time is unlikely in a real system, but as the objective of this paper is to provide a theoretical description of the different facets of this specific sub-case of zero-missing phenomenon, the shorter extinction time is still considered. Future work in this topic will limit the analysis to realistic cases, in order to better assess the risks to the system.

Table I. Initial DC current [A] for a SFTG fault and a clearing time of 40ms (left) and 105ms (right) at different distance of S_B

	Simul	Eq (1)	Eq (3)		Simul	Eq (1)	Eq (3)
0km	-140	-99	-146		-461	-547	-494
5km	-123	-84	-131		-410	-497	-445
10km	-110	-72	-120		-369	-447	-394

The current during a fault is inductive-resistive lagging the voltage, with the exact phase-difference depending on the system parameters, mainly lines and transformers. In the event of a fault with decaying DC current, the phase-difference depends also on the opening time of the CB. Fig. 4 shows a phasor representation of the fault current (red), plus the voltage (blue) and current (green) at one SR, as well as the impact of performing the angle correction in (3), all at the fault extinction instant. Additionally, the initial magnitude of the DC current in the SR is shown considering both a case where the SR is deenergised, i.e. alike a normal energisation or if the fault occur at the SR current crossing 0A (crosses), and a case where the fault instant is for peak current (crosses inside circle). Notice that both consider the DC current of the fault fully damped at the fault extinction instant and the magnitudes are not at scale. For a better interpretation, I_{SR_DC} (cross inside of circle) is equal to I_{SR_FC} (red circle) plus -I_{SR_AC} (cross), with the left figure showing the quantities for a fault extinction time of 105ms, whereas the right figures shows for 40ms.

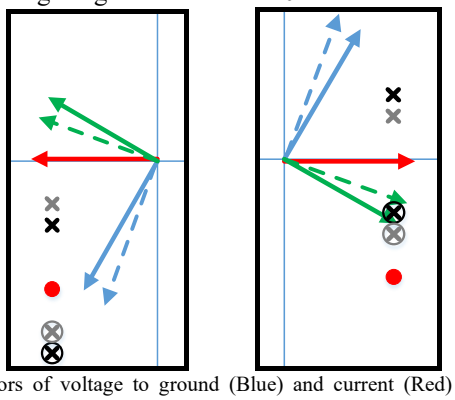

Fig. 4. Phasors of voltage to ground (Blue) and current (Red) at CB, AC component of current in SR (Green), current in SR prior to fault extinction (Red circle). Solid line: Using (1); Dashed Line: Using (3). Crosses: Initial SR DC current if deenergised; Crosses inside circle: Initial DC current a SR if fault at peak current. Left: Extinction time of 105ms; Right: Extinction time of 40ms

The phasor representation allows concluding that the polarity of the voltage at the extinction instant affects I_{SR_DC}. If the polarity of voltage and current at the SR during the fault is the same when the CB opens (Fig. 4-Left), the initial DC current is larger than if the polarities are opposite (Fig. 4-Right). The former may even lead to a DC current larger than the worst-case at a normal energisation, depending on the fault instant (i.e. I_{SR_FC}). This is the case for the clearing time of 105ms, where an I_{SR_DC} of -461A is 110A larger than the maximum initial DC current for an energisation. Table I quantifies the effect of the polarity for the two extinction times.

The phasor representation in Fig. 4 does not consider the fault decaying DC component (I_{F_DC}) that may be present during the first cycles of the fault has a beneficial impact reducing I_{SR_DC} for the worst-case scenario (i.e. maximum I_{SR_FC}). As faults are usually inductive, the I_{F_DC} has a polarity opposite to I_{SR_FC} leading to the scenario presented in Fig. 5, which is equivalent Fig. 4, but with a random value for I_{F_DC}. The arrow indicates the impact of an increasing I_{F_DC} in the phasors. Therefore, if the voltage at the extinction instant without considering the impact of I_{F_DC} has the same polarity of I_{SR_FC}, there is a delay, which means one of two things:

- the voltage is in the same quadrant, I_{SR_AC} reduces magnitude;
- the voltage goes to the next quadrant, I_{SR_AC} increases in magnitude, but with opposite polarity.

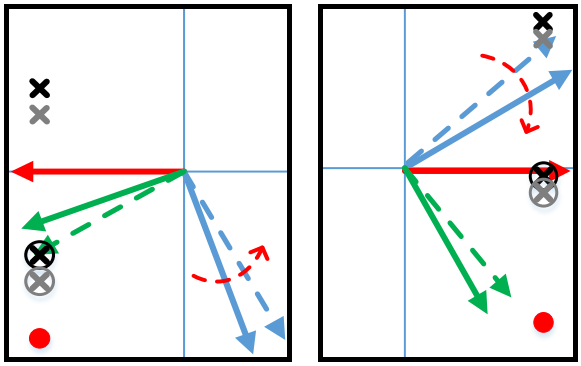

Fig. 5. The figures corresponds to Fig. 4, but considering that the fault decaying DC component is not damped before fault extinction. The arrow indicates the impact of an increasing *IF_DC*

Both cases mean a reduction of I_{SR_DC} when compared with a case where the fault DC component is zero. Fig. 5-Left shows this case for maximum I_{SR_FC} and the observation of the vectors could indicate that if I_{SR_FC} is small (red circle near horizontal axis), and the voltage enters in the next quadrant, I_{SR_DC} increases when compared with a scenario where fault DC current is null. However, as a SR is inductive and a fault is mostly inductive, to have a low I_{SR_FC}, it means a low fault DC current and thus, this case is of little impact.

If the voltage at the extinction instant with I_{F_DC} damped had equal polarity to I_{SR_FC}, there is an advance, which increases the magnitude of I_{SR_AC} with opposing polarity to I_{SR_FC}, reducing the value of I_{SR_DC}. This is the case for the fault clearing at 40ms, which has a lower I_{SR_DC} than for the fault clearing time of 105ms, both because of the polarity of the voltage at extinction instant and the DC fault current: As an example, I_{SR_DC} would be -155A, instead of -140A, for a clearing time of 100ms, which has the same voltage polarity, but a lower I_{F_DC}.

Fig. 4 also shows how (1) underestimates I_{SR_DC} for 40ms, overestimating it for 105ms. The black and grey crosses within circles are for (1) and (3), respectively, with Fig. 4-left representing a scenario similar to the 105ms clearing time and Fig. 4-right to 40ms. The former sees the cross within circle with a higher vertical displacement for (1) than (3), with the opposite occurring for the later, justifying the results at Table I.

IV. Impact of Different System Layouts

A. Transformer connected at substation

The system complexity increases and the system becomes more realistic, by considering an autotransformer connected at SB_B (Fig. 6). The explanations regarding the phenomenon behaviour from the previous section remain valid, with the autotransformer affecting the magnitude of the current at the SRs during the fault and the ramp of the voltage at SB_B after fault clearing, both affecting the value of θ_l. The estimation of θ_l is done using LC elements (Fig. 7). Seen from S_{BB}, the resonance frequency is given by (5), where L_{SR} is the parallel inductance of all SR connected to the busbar.

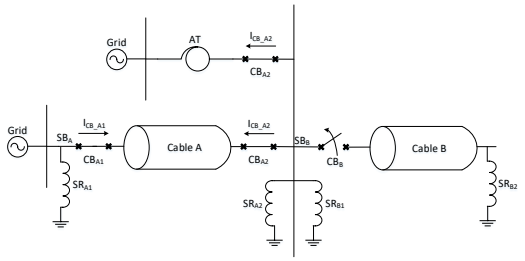

Fig. 6. Single-line diagram of system with two cable and an autotransformer

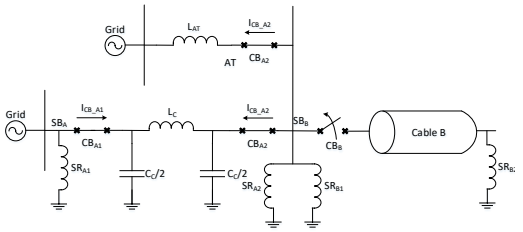

Fig. 7. LC equivalent of Fig. 6 circuit

$$\omega = \sqrt{\frac{L_{AT}L_{SR} + L_C L_{SR} + L_{AT}L_C}{L_{AT}L_{SR}L_C \frac{C_C}{2}}} \quad (5)$$

After fault clearing, the voltage at SB_B starts oscillating reaching the source voltage instantaneous magnitude after a time t calculated by (6) and converted into an angle by (7).

$$V_G \sin(\theta_{FC}) = V_G \cos(\omega t) \pm V_G \Leftrightarrow t = \frac{\cos^{-1}(\sin(\theta_{FC}) \mp 1)}{\omega} \quad (6)$$

$$\theta_l = t\frac{2\pi}{T} \quad (7)$$

Table II shows simulation and the estimation of the SR_{B1} initial DC current using this method, showing the same tendencies from the previous section.

Table II. Initial DC current [A] for a SFTG fault and a clearing time of 40ms (left) and 105ms (right) at different distance of S_B

	Simul	Eq (1)	Eq (3)		Simul	Eq (1)	Eq (3)
0km	-148	-104	-146		-327	-426	-384
5km	-98	-49	-91		-226	-318	-276

10km	-70	-16	-58		-176	-255	-214

This approach can be used for any system by considering the inductances and capacitances in parallel. If the network is weak, an error is introduced when using this methodology, which can be minimised by adding the Thévenin inductance at the busbar in series with the equipment's inductance, per example: L_{Th} at SB_A with L_C. However, the weaker the network, the less likely is zero-missing to occur at fault disconnection and the worst-case happens for maximum network strength.

V. Other Impacts from the System

A. Short-circuit power

The network strength affects the initial DC current, by affecting the ramping of the voltage. As shown in Fig. 4, this can increase or decrease the initial magnitude of the DC current depending on the voltage polarity. For the worst-case scenario, the larger the short-circuit power, the larger the initial DC current. This can be seen in Fig. 4-left, by comparing the grey and black crosses within a circle, with the black corresponding to a stronger grid. Regarding the use of (3), the estimation of θ_l is a source of error, whose error decreases the stronger the grid seen from the busbar, because of the value of the angle becomes lower. As an example, if the leakage reactance of the autotransformer was half, the estimated I_{SR_DC} for the 0km and 105ms clearing time would be -378A and the simulated -350A, as error of 28A instead of 57A. Likewise, the error would decrease if the cable was shorter, if more cables where in parallel or by other factors that increased the network strength.

B. Grounding resistance of cable sheaths

The previous results and methodology are for a solid grounding of the sheaths and both-ends bonding at Cable A. A faster damping of the DC current due to the sheaths' grounding resistances is not considered. Typically, substations have grounding grids for assuring an equal grounding potential at the substation. The cable's sheath connects to the grounding grid, which is equivalent to solid grounding of the sheaths. If such connection does not exist, the DC current from the SR flows to the ground and partially into the cable's sheath via the grounding resistance and out of the sheath at the other end. In this case, the grounding resistance damps the DC current, reducing the severity of the phenomenon. Given that grounding grids are commonly used and lead to a longer phenomenon duration, only this design is considered in this paper.

C. Fault resistance

All previous results have been presented for a solid fault. The fault impedance influences the DC current at fault clearing in two ways, both leading to its reduction:

- Damping of current during the fault: I_{SR_FC} becomes smaller;
- AC oscillation of I_{SR_FC} during the fault, similar to the impact of having the fault at a certain distance from the busbar;

A fault has always a certain impedance, but to consider solid faults might not introduce a large error, as faults at substations can have a very low impedance: a typical case is to forget to open the ground disconnector after maintenance work. Thus, the simulation of a solid fault provides a safety margin when assessing the phenomenon, which is not exaggerated.

D. Amount of reactive power compensation

The amount of reactive power compensated via SRs connected directly at the busbar varies depending on the system layout and the TSO procedures. Compensation of 50% or more directly at the cable is not typical, with the majority of the compensation being made at substations. Ideally, the reactive power compensation would be equal at the two ends of a cable, but practical considerations may result in other arrangements.

If two cables are connected to a substation, as shown in Fig. 1 or Fig. 6, zero-missing depends on the combination between the AC current of the Cable A with the AC and DC current of the various SRs. Fig. 8 shows the zero-missing current at CB_{A1} as a percentage of the AC current for different reactive power compensation levels at the substation and different lengths of Cable B, considering the DC current equal to the peak AC current. Both SRs compensate an equal percentage for the respective cables (20% compensation means 20% of reactive power compensation for Cable A and 20% for Cable B) and the length of Cable B varies between half and four times the length of Cable A. A negative value in the vertical scale means that the AC current is larger than the initial DC current, whereas a positive value means the opposite and zero-missing is present. The results tend to infinite when the AC component tends to 0A and the vertical scale is limited to 300%. Fig. 8 shows that if Cable B is long in relation to Cable A and the reactive power compensation of both is made at the busbar, zero-missing may occur for low reactive power compensation levels.

Fig. 8 results are for an initial DC current equal to the peak AC current. The initial DC current can be larger, as previously proven, increasing the duration of zero-missing and leading to the phenomenon at lower compensation levels.

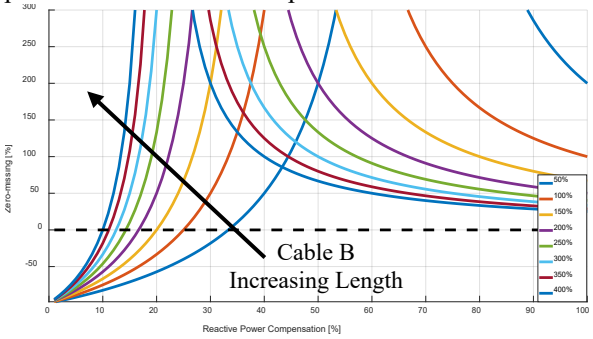

Fig. 8. DC current in percentage of AC current for different reactive power compensation levels and different cable lengths, considering initial DC current equal to peak AC current

E. Worst-Case Scenario

Based on the results previously obtained and theoretical explanations, the worst-case scenario consist in:

- A solid fault occurring at the substation;
- The fault occurs for voltage crossing 0V, which leads to a current at the SR(s) during the fault with a magnitude almost equal to the AC peak value;
- The DC fault current is damped before opening the CB;
- The CB opens when the voltage has the same polarity of the current in the SR during the fault;
- A high short-circuit power at the busbar;

• Solid grounding of the cable's sheaths;

These conditions lead to maximum initial DC current from the SR(s) and thus, longer zero-missing, if present. The fault instant is random and a solid fault at the substation would likely be caused by a human error, the polarity of the voltage at opening is 50/50 and the last two bullet points are not unusual. The simulation of this sub-case of zero-missing can be seen similar to statistical switching, but with varying fault instants.

F. Estimation of I_{SR_FC} and θ_{FC} for worst-case scenario

The values in Table I and Table II used simulations to estimate I_{SR_FC} and θ_{FC} for input in (2) and (3). Whereas the formula is useful to explain the phenomenon, it is in these conditions useless for practical applications, as one would simply use the simulation to obtain the initial DC current. In practice, these two values can be also estimated with simple equations for solid faults at the busbar.

The angle θ_{FC} is estimated by (8), assuming that current chopping, DC fault current and/or reignitions/restrikes are not present. The L_{eq} and R_{eq} are the Thévenin equivalents seen from the node, not considering the faulted cable. The DC fault current is not consider, because it reduces I_{SR_DC}, with the exception being for cases with small I_{SR_DC}, as previously shown.

$$\theta_{FC} = \tan^{-1}\left(\frac{2\pi L_{eq}}{R_{eq}}\right) \tag{8}$$

I_{SR_FC} is a random value between the positive and negative peak values of the AC current at the SR, which depends on the fault instant and location. The current I_{SR_FC} during the fault is given by (9). This also means that I_{SR_FC} can never be larger than I_{SR}, as I_{CB_B} is always smaller than I_{SR}. Equation (9) is valid only for solid faults at the busbar and the worst-case corresponds to an angle of 90° or 270°.

$$I_{SR\_FC} = I_{SR}\sin\left(\theta_{FC}\right) \tag{9}$$

VI. Countermeasures

Several countermeasures are described in the literature [1]-[4] to avoid zero-missing at energisation, but many are ineffective for zero-missing at fault clearing, as per example: Controllable switching instant, use of a pre-insertion resistor, energisation of cable and SR at different instants. One countermeasure efficient to avoid zero-missing at both energisation and fault clearing is the installation of a resistance in series with the SR, i.e. lower X/R ratio, which would accelerate the damping of the DC current. However, it also means permanent losses and it is rarely used.

A possible countermeasure to avoid zero-missing at fault clearing is the coordination of the protection system. The relay disconnecting the faulted cable sends an additional trigger signal for the CB of the SR at the busbar, eliminating the DC current from the system. The disconnection of the SR may also be required, in order to avoid voltage drop, because of excessive reactive power consumption. However, this countermeasure presents a challenge, as the CB of the SR may also face zero-missing. This is impossible for an energisation, but for fault clearing, the DC current of the SR may be larger than the peak AC current, as previously shown.

The disconnection of the SR may result of other problems as current chopping, which is more prone in disconnection of small inductive loads. If current chopping occurs, one would risk superimposing a second voltage transient to the one occurring at disconnection, potential increasing the risk of reignition. The current in the SR is not a small inductive current, but as far as the authors can see, no research exists on the impact that a DC current superimposed on the inductive current has on current chopping. In case of problems with current chopping, an option could be to have a CB opening time controlled, so that the switching arc conducts until current zero crossing [6] or an oil circuit breaker. Another challenge of this countermeasure is that multiple SR may be installed at the substation and it may not be feasible to disconnect them, because it would lead to an overvoltage. A single SR with different compensation levels may be used instead, and the same problem is faced.

VII. Discussion

The work presented in this paper demonstrated that zero-missing after fault clearing is a possibility. This case is not accounted for at system design, with zero-missing analysis limited to energisation. Furthermore, the initial magnitude of the DC current at the SR may be larger than the respective peak AC current, something impossible for a normal energisation, and the reactive power compensated at the busbar after fault clearing is larger than the one generated by connected the cable(s). As a result, the duration of zero-missing might be longer than for an energisation. Finally, the countermeasures used to avoid the phenomenon for energisation are ineffective.

Zero-missing phenomenon is not a problem on itself. It is unwanted during energisation, because it is not possible to open the CB if necessary, as in case of an asymmetric fault. A similar situation for the sub-case studied in this paper considering the circuit in Fig. 6, it would be to have an asymmetric fault in Cable A after clearing a first fault that lead to zero-missing. Such is unlikely to happen, but possible. A problem specific for the fault clearing zero-missing is that the current through the CB of the SR may also experience zero-missing, something that does not happen at energisation zero-missing. As a result, it might not be possible to disconnect the SR(s) for some cycles while it consumes reactive power that is no longer generated by the cable and potentially affecting the voltage level and the flow of reactive power in the system.

A special countermeasure potentially valid for this case, but not for energisation, would be to coordinate the protection system so that the CB of the SR receives a trigger signal from the relay of the faulted cable. However, the applicability of this countermeasure may be challenging when several SRs are installed at the substation and/or taps are used, as the simultaneous disconnection of the SRs may initiate a large transient with a negative impact in the system.

It was not demonstrated in detail, but the fault impedance, including the arc in the circuit breaker impacts the damping of the SR current during the fault, leading to a smaller initial DC current at fault clearing. The same happens the further away the fault is from the busbar, because of series resistance, reducing the severity of the phenomenon and it may even eliminate it.

The worst-case is for a solid fault at the busbar occurring

when the voltage crosses zero. A perfect solid fault is impossible, but a similar scenario is the forgetfulness of removing flexible safety grounding after maintenance or reparations. Equations are provided for a fault estimation of the DC current in the SRs for this scenario that can be used to perform a basic risk assessment by varying the fault instant.

The analysis considers that the grounding of the SR and cable's sheaths is common, with negligible resistance in between, emulating the grounding grid of a substation. If such is not the case and a grounding resistance is present in the current loop, a faster damping of the DC current exists, reducing the severity of the phenomenon.

The three topics introduced next are relevant for the analysis of the phenomenon and they will be researched in future work. The first two may show that zero-missing after fault clearing is not a problem in a conventional grid, whereas the third may show an increase probability of wrongful operation.

As previously stated, zero-missing is unwanted, because it is not possible to open a circuit breaker if necessary, as in case of asymmetric fault. However, it is possible that such fault generates an AC current larger than the DC current at both the faulted and sound phases. The faulted phase might connect to the sound phases at the autotransformer, per example as in Fig. 6, which might lead to an increase of the AC current in the sound phases large enough to allow disconnecting the CB. This means that the increase of the AC current depends on the system layout and fault impedance, per example. Additionally, load current is expected to be present after fault clearing, increasing the magnitude of the AC current component at the CB.

The second topic requiring more research is the impact of the electric arc in the CB during the fault. The simulations and analysis in this paper were for solid faults and ideal CB, neglecting the impact of the arc and fault impedances. The disregarding of the latter can be acceptable, as previously explained, but the impact of the former should be assessed.

The third topic requiring research is the saturation of the current transformers because of the DC current. Depending on the fault instant, the magnitude of the DC current may be larger than the maximum DC current from an energisation, increasing the risk of saturation of the current transformers and thus, affecting the efficiency of the protection relays. Generally, saturation of a CT due to DC current takes some cycles [7], and thus, the exact impact of this extra DC current present for several seconds must be studied. However, this is typically not a problem for modern saturation insensitive relays.

In summary, future work will asset the consequences of this type of zero-missing and provide a practical approach by researching the following topics:

- To have zero-missing phenomenon due to fault clearing may not be an issue, because the current in the sounded phases during an asymmetric fault might also cross 0A;
- The arc in the CB may damp part of the DC current reducing the severity of the phenomenon;
- Impact of higher DC current in saturation of a CT;
- The challenges of the proposed countermeasure;
- Based on this work, it is likely that reignitions/restrikes during the opening of a CB of a SR have an impact in the phenomenon;

VIII. CONCLUSIONS

Conventionally, zero-missing phenomenon is linked with the energisation of a cable and shunt reactor simultaneously. This paper demonstrated that zero-missing phenomenon might also occur after clearing a fault at a substation or in its vicinity. Moreover, the initial DC current at the shunt reactor causing zero-missing may be larger than the peak AC current at the shunt reactor, something impossible for an energisation, making it impossible to disconnect the shunt reactor during several cycles. It is also demonstrated that the countermeasures used to avoid zero-missing at energisation are ineffective, except for the installation of a permanent resistor, which would lead to permanent losses.

Future work will study this sub-case of zero-missing phenomenon in more detail, to evaluate and to quantify the risks that it may pose for a transmission grid.

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X. APPENDIX

A. Simulation Data

All simulations were done in PSCAD/EMTDC. The cables were modelled using frequency-dependent phase models, in trefoil formation and the data in Table 3. The shunt reactor was modelled via an ideal inductor. The fault was simulated via the switching of a 10μΩ resistance (solid fault) between the busbar and the ground.

Table 3 – Cable data

Layer	Radius (mm)	Properties
Conductor	22.57	$\rho=3.156\text{x}10^{-8}$ [Ω.m]
Insulation	41.1	$\varepsilon_r=3$
Screen	42.81	$\rho=4.8939\text{x}10^{-8}$ [Ω.m]
Outer Insulation	47.5	$\varepsilon_r=2.3$