HIL Testing of an LCC-MMC Multi-terminal HVDC System in Various Operating Modes

Zhe Zhu, Wenming Gong, Jun Chen, Fei Zhang, Weihua Wang, Wei Li

***Abstract*—An HVDC system composed of the line commutated converter (LCC) in the rectifier side and the modular multilevel converter (MMC) in the inverter side can take advantage of both technologies. A three-terminal HVDC system with one LCC and two MMC terminals is planned to connect grids of Yunnan, Guangdong, and Guangxi, in China Southern Power Grid (CSG). In this HVDC system, the MMC terminals are composed of hybrid half bridge submodules (HBSMs) and full bridge submodules (FBSMs) for the fault right-through and on-line valve switching purpose. This paper explains how the system is designed and some key parameters, e.g. the ratio of FBSM, are selected to improve the system economy and reliability. The modelling methodology of MMC with hybrid SMs to achieve real time performance is presented in this paper. The system is simulated and validated with a hardware-in-the-loop (HIL) test bench and connected to manufacturer's controller replicas. HIL test results are presented showing the LCC-MMC multi-terminal hybrid HVDC system can operate at various operating modes.**

***Keywords*: Line commutated converter; Modular multilevel converter; Multi-terminal HVDC; Real-time simulation.**

I. Introduction

THE line commutated converter (LCC) is a mature technology that has been widely applied in HVDC transmission systems due to its advantages of high reliability, high power transmission capability, and low cost. However, the commutation failure of the LCC-HVDC largely affects the system stability. Voltage source converter (VSC) based HVDC system has the advantages of independent control of active and reactive powers, capability of black start and connection to week AC grid [1]. Among existing VSC topologies, modular multilevel converter (MMC) is a promising topology, which offers benefits including high efficiency, modular design, and no filter requirement [2].

The development of HVDC system is switching from point to point connection to multi-terminal grids. The hybrid HVDC system with LCC-MMC can take the advantages of both technologies [3]. China Southern Power Grid (CSG) plans to build a three-terminal HVDC system that transmits the hydropower from generation in Wu Dong De (WDD), Yunnan Province to the load centers in Guangdong and Guangxi Provinces, as described in Fig. 1. The DC bus will be rated at ±800 kV, and the transmission distance is around 1476 km. The power ratings are 8000 MW at the source side, 5000 MW and 3000 MW, for Guangdong Province and Guangxi Province respectively at the two load sides. The rectifier that connects to the hydropower adopts the LCC technology since the issue of commutation failure rarely happens at this side. Both the inverters at the load side use the MMC technology. The LCC-MMC system is required to operate at a reduced DC bus voltage during AC fault. The MMC can reduce the DC bus voltage to assure the power transmission. Moreover, the MMC also has the capability to assist the recovery process of the AC fault.

The LCC-MMC system should be capable to ride through DC faults, which is a critical requirement for HVDC systems with overhead power lines. Unlike LCC, the MMC with half bridge submodules (HBSMs) is not able to block the DC fault since the fault current can still conducting from AC side to the DC side through the diodes of SMs. One solution, the dc breaker, is still too expensive and not mature in current stage. Alternatively, new types of SM, including the full bridge submodules (FBSMs) and clamp double submodules (CDSMs), have been proposed to solve this issue [4]-[6]. Among them, the FBSMs are preferred since the MMC can continue to operate without blocking the switches and work as a synchronous compensator (STATCOM) to support the AC grid during DC fault. However, the MMC with FBSMs has double the number of switches, which increases the system cost and loss. To address this issue, the hybrid MMC composed of HBSMs and FBSMs are discussed in [7]-[9].

The design of the MMC should meet all the requirements mentioned above including stable power transmission at a reduced DC bus voltage, reactive power supply during AC fault, DC fault ride through, etc. The ratio of the FBSMs in the MMC arm should be carefully selected to reduce the chance of

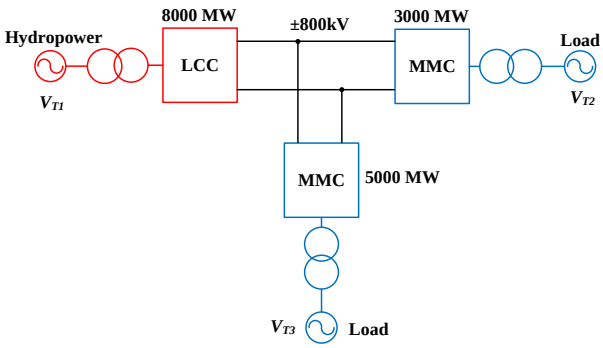


Fig. 1. Kun Liu Long (KLL) three-terminal hybrid HVDC system.

This work was supported by the National key research and development plan "2016YFB0901000", China.

Z. Zhu, W. Gong, and J. Chen is with Electric Power Research Institute (State Key Laboratory of HVDC), China Southern Power Grid, China (e-mail of corresponding author: zhuzhe@csg.cn).

F. Zhang, W. Wang, and W. Li is with OPAL-RT Technologies, Montreal, Canada (e-mail: fei.zhang@opal-rt.com).

Paper submitted to the International Conference on Power Systems Transients (IPST2019) in Perpignan, France June 17-20, 2019.

multi-commutation failure. The design principles of the LCC-MMC hybrid HVDC system are discussed in this paper. A modelling methodology of the MMC that can simulate the hybrid SMs in real-time is also presented. Hardware-in-the-loop (HIL) test is carried out to validate the system performance during different test scenarios.

II. Design Principles

The configuration of the LCC terminal is the double 12-pulse thyristor bridge, which has a rating of 400 kV. The MMC terminal can be configured by either single MMC valve or double MMC valves per pole. The configuration with double MMC valves per pole is described in Fig. 2, where each pole consists of two MMC valves, namely the upper valve and the lower valve. In the case where one of the LCC rectifiers is required to be switched-out, the MMC side should be able to work at 50% reduced dc voltage. Therefore, the MMC should be designed with the capability to switch the valve on-line, which is to switch-out the valve from 800kV to 400kV per pole and switch-in the valve from 400kV to 800kV per pole.

The LCC terminal can block the DC fault by operating at the inverter mode. To block the DC fault for terminals with MMC, the MMC arm is composed by HBSMs and FBSMs. The ratio of the FBSMs should meet the requirements including DC fault blocking capability, capacitor voltage balancing between HBSMs and FBSMs, and reduced DC bus voltage operation.

The nominal DC component voltage of each MMC arm in the double series-connected configuration is defined as

$$V^*_{arm\_DC} = \frac{V_{DC}}{2k} \tag{1}$$

where k is the number of MMC valve per phase (k=4 for the configuration of double valves per pole).

The arm voltage and arm current can be expressed as

$$v_{arm} = V_{arm\_DC} + v_{arm\_AC} \tag{2}$$

$$i_{arm} = I_{arm\_DC} + i_{arm\_AC} \tag{3}$$

where $V_{\text{arm\_DC}}$ and $I_{\text{arm\_DC}}$ are the DC component of arm voltage and current, respectively. $v_{\text{arm\_AC}}$ and $i_{\text{arm\_AC}}$ are the AC component of arm voltage and current, respectively.

The amplitude of arm AC component voltage can be

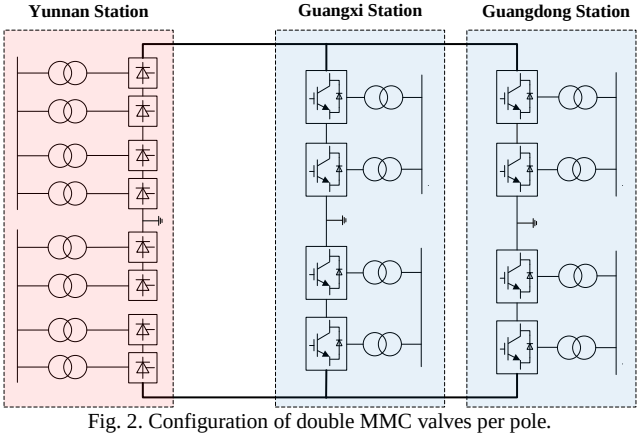
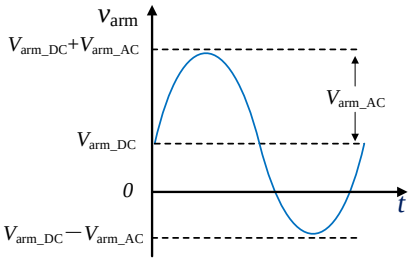
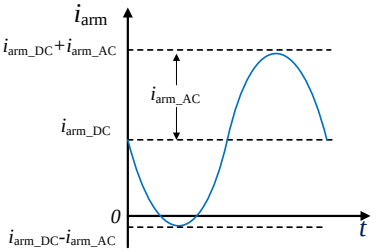


Fig. 2. Configuration of double MMC valves per pole.



(a) arm voltage



(b) arm current

Fig. 3. MMC arm voltage and current under recued DC voltage.

defined as

$$V_{arm\_AC} = M \cdot V^*_{arm\_DC} \tag{4}$$

where M is the modulation index.

During steady-state, the arm energy should be balanced, where the AC and DC power exchanged in the arm can be expressed as

$$\frac{1}{2} V_{arm\_AC} \cdot I_{arm\_AC} . \cos(\theta) = V_{arm\_DC} \cdot I_{arm\_DC} \tag{5}$$

where θ is the phase shift between arm AC voltage and AC current. $I_{\text{arm\_AC}}$ is the amplitude of AC component of arm current.

The amplitude of the AC current is calculated as

$$I_{arm\_AC} = \frac{2}{3M \cdot \cos(\theta)} \cdot \frac{V_{arm\_DC}}{V^*_{arm\_DC}} \cdot I_{DC} \tag{6}$$

where I_{DC} is the DC bus current that is three times of $I_{\text{arm\_DC}}$.

To balance the capacitor voltage of HBSMs, the arm current should have negative part as described in Fig. 3. Otherwise, the capacitor voltage of HBSMs will keep increasing since the output voltage of the HBSMs is non-negative. In Fig. 3, it should be noted that all the positive arm voltage can be generated by HBSMs and FBSMs, while the negative arm voltage is generated only by FBSMs. From (3) and (6), the following requirement can be derived

$$-\frac{2}{3M \cdot \cos(\theta)} \cdot \frac{V_{arm\_DC}}{V^*_{arm\_DC}} \cdot I_{DC} + \frac{1}{3} I_{DC} < 0 \tag{7}$$

From (7), the minimum $V_{\text{arm\_DC}}$ can be calculated as

$$V_{arm\_DC} = \frac{M \cdot \cos(\theta) \cdot V^*_{arm\_DC}}{2} \tag{8}$$

For the case that the system is required to operate at a reduced DC voltage, the amplitude of the AC component voltage should still maintain close to its nominal value, in which case M is usually around 0.85-1 (M can be higher than 1 for the hybrid MMC arm). Therefore, assuming the MMC arm operates at near unity power factor, the minimum DC bus voltage that the HBSMs can still maintain balanced is around

50% of its nominal value. An alternative way to make the system operate at a DC voltage lower than the minimum value is to increase the percentage of the FBSM in the arm, which is simpler and more straightforward than injecting reactive power or circulating current on purpose to make the arm current have negative value in one cycle. In this case, all the HBSMs are bypassed and the arm voltage is generated only by FBSMs

$$V_{arm\_FBSM} = V_{arm\_DC} + V_{arm\_AC} \tag{9}$$

The percentage of FBSMs prt_{FBSM} required can be calculated from (4), (8), and (9)

$$prt_{FBSM} = \frac{V_{arm\_DC} + V_{arm\_AC}}{2V^{*}_{arm\_DC}} = \frac{(\cos(\theta)+2)M}{4} \tag{10}$$

To enable the capability of on-line valve switching and operation during fault, the system should be capable of operating at 50% DC bus voltage or lower, then prt_{FBSM} is recommend as 70%.

III. Modelling of the LCC-MMC Hybrid HVDC System

Real-time simulation of the LCC-MMC hybrid HVDC system can be implemented on central processing units (CPUs) and field programmable gate arrays (FPGAs). Subsystems with slow dynamics are implemented on CPU, while the subsystems with fast dynamics are implemented on FPGA. The MMC valve model is implemented on FPGA that has a time-step of hundreds of nanoseconds to guarantee the high accuracy and reduce the latency and delay. Each individual SM can be simplified as an equivalent circuit consists of two ideal diodes and two voltage sources [10]. The MMC arm with hybrid HBSMs and FBSMs can also be represented by an equivalent circuit as described in Fig. 4. In Fig.4, D_1 and D_2 are ideal diodes, $V_{sp\_\Sigma HB}$ and $V_{sn\_\Sigma HB}$ are the summation of source voltages of HBSMs which represents the capacitor voltage and forward conduction voltages of diodes and IGBTs. $V_{sp\_\Sigma HB}$ and $V_{sn\_\Sigma HB}$, representing the source voltages in the positive and negative current direction respectively, are the summation of source voltages of HBSMs accordingly. All the hybrid SMs connected in series can be simplified as a valve equivalent circuit as described in Fig. 4. The source voltages of the valve equivalent circuit are the summation of all the HBSM and FBSM source voltages, which are calculated as

$$V_{sp\Sigma} = V_{sp\_\Sigma HB} + V_{sp\_\Sigma FB} \tag{11}$$

$$V_{sn\Sigma} = V_{sn\_\Sigma HB} + V_{sn\_\Sigma FB} \tag{12}$$

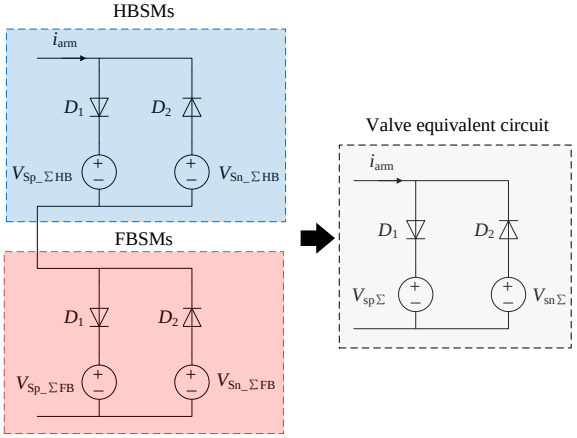


Fig. 4. Equivalent circuit of MMC with hybrid SMs.

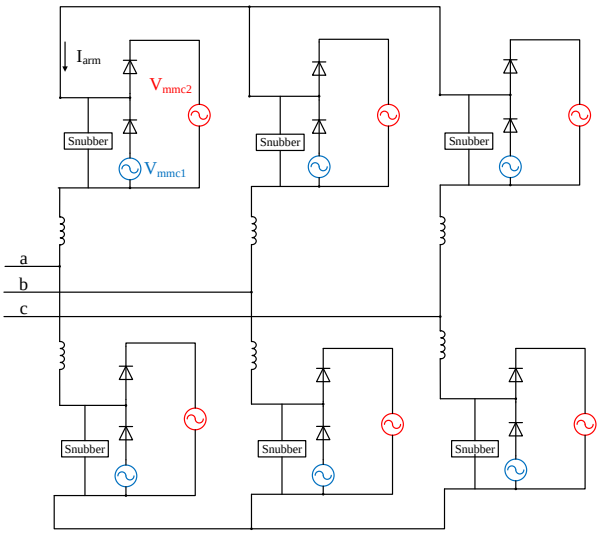


Fig. 5. MMC subsystem implemented on CPU.

The MMC subsystem on CPU is described in Fig. 5, where V_{mmc1} and V_{mmc2} are the valve voltages of the hybrid SMs calculated on FPGA by (11) and (12). The real-time simulation system is presented in Fig. 6, where the plant is connected to an external controller. The LCC subsystem and MMC subsystem are implemented on CPU, while the MMC valve model is implemented on FPGA. The arm currents are sent from CPU to FPGA, while the MMC valve voltage and capacitor voltages are sent from FPGA to CPU. The whole plant system is simulated by multi-rate that is decoupled by the transmission line.

IV. Performance Results

In this section, the LCC-MMC three-terminal Hybrid HVDC system is simulated and validated in a HIL test bench. The system is implemented on OPAL-RT Technologies real-time simulator OP5600 and OP5607, which is connected to manufacturer's controller replicas as described in Fig. 7. The

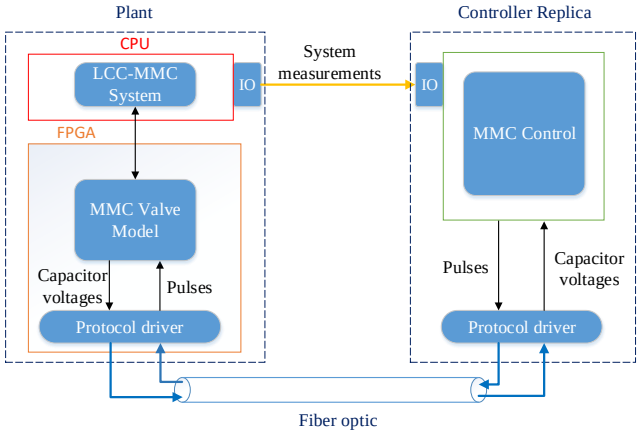


Fig. 6. Plant configuration for HIL test.

Table I. System parameters

Parameter	Symbol	Value
CPU Time-step	T_s	50 μs
Power rating	P	1000*8 MW (Yunnan) 1250*4 MW (Guangdong) 750*4 MW (Guangxi)
Primary voltage	V_{prim}	525 kV
Secondary voltage	V_{sec}	244 kV (Guangdong) 220 kV (Guangxi)
DC voltage	V_{dc}	±200 kV
Frequency	f	50 Hz
Number of SMs per arm	N	216 (176 FBSM, 40 HBSM)
Startup resistor	R_{start}	5000 Ω
Arm inductor	L_1	40 mH (Guangdong) 55 mH (Guangxi)
Arm SM capacitance	C_{sm}	18 mF (Guangdong) 12 mF (Guangxi)

parameters of the test system are shown in Table I. The time-step of the model running on CPU is 50 μs, while the time-step of MMC valve implemented on FPGAs are 250 ns. Several test scenarios including MMC start-up, AC fault ride-through and DC fault ride-through are carried out. All the results are shown in p.u. value.

A. MMC Start-up Test

The results of MMC start-up test is presented in Fig. 8. After the AC breaker closed at t=54 s, the capacitors of FBSMs and HBSMs are charged to different voltages by natural diode charging due to the conduction times are different. At t=63 s, the voltage balancing control of SMs is applied, then the capacitors of FBSMs and HBSMs are controlled to the same voltage. The start-up resistor is bypassed at t=88 s and the pulses of MMC are applied at t=100 s. The DC bus voltage and the capacitor voltages of FBSMs and HBSMs are all controlled to their nominal values. From Fig. 8, the MMC has a smooth start-up, while no inrush current or voltage is observed.

B. AC Fault Ride-through Test

In this test scenario, the MMC2 controls the DC bus voltage, while LCC and MMC1 control the active power. A three-phase to ground fault is applied at MMC1 and it lasts for 0.5 s. As described in Fig. 9, the three-phase to ground fault is

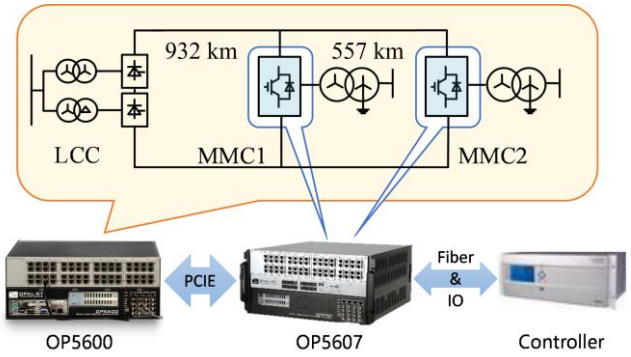
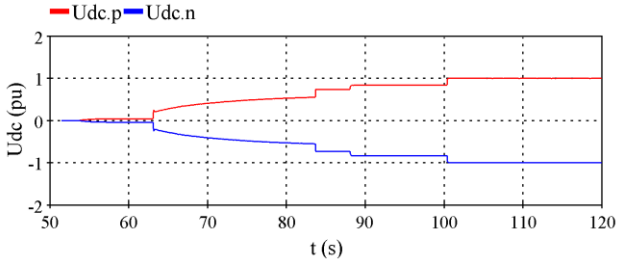
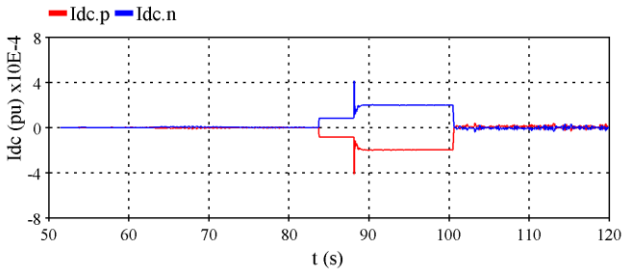


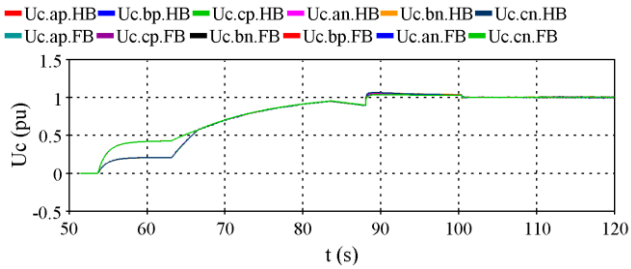
Fig. 7. HIL test bench of an LCC-MMC hybrid HVDC system.



(a) DC voltage

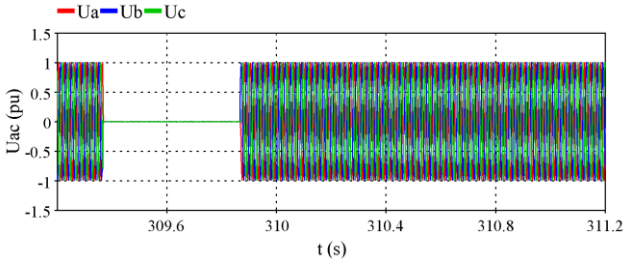


(b) DC current

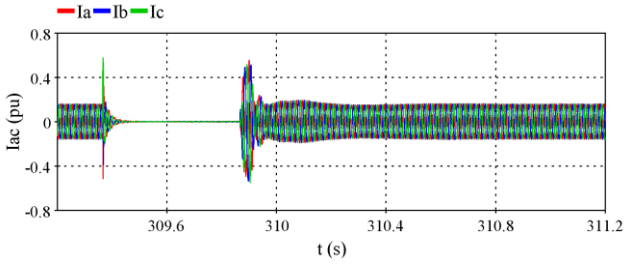


(c) Average capacitor voltage of SMs

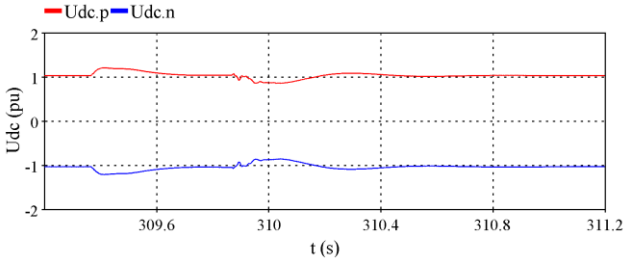
Fig. 8. Strat-up test of MMC.



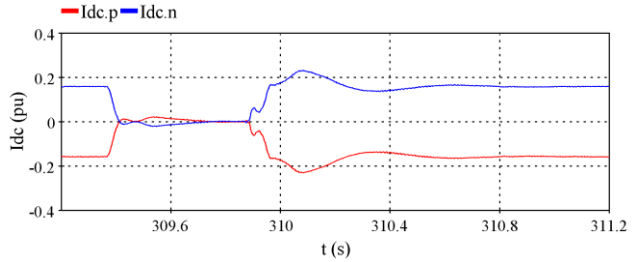
(a) AC voltage of MMC1



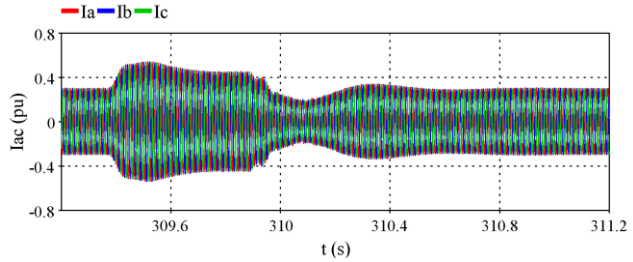
(b) AC current of MMC1



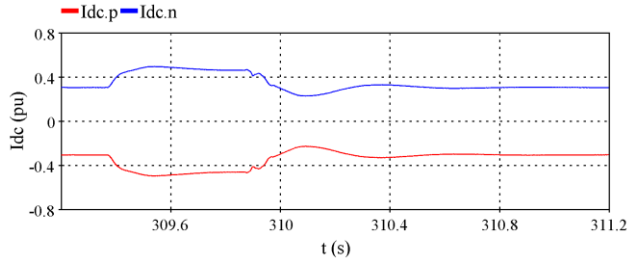
(c) DC voltage of MMC1



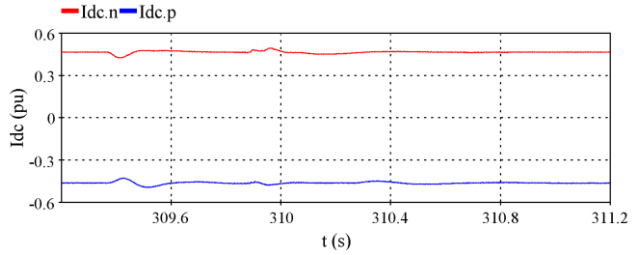
(d) DC current of MMC1



(e) AC current of MMC2



(f) DC current of MMC2



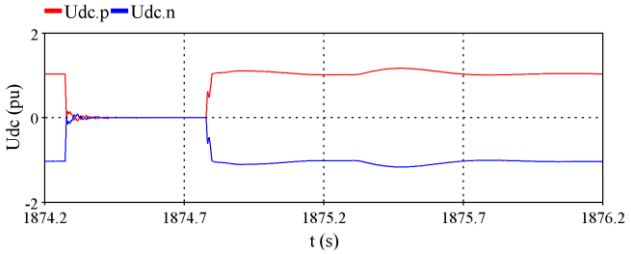
(g) DC current of LCC

Fig. 9. AC fault ride-through test of the three-terminal hybrid HVDC.

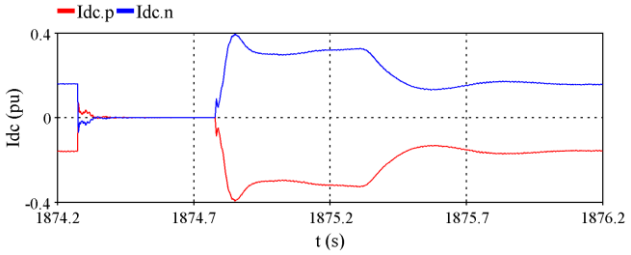
applied at MMC1 near *t*=309.3 s. The power received by MMC1 is shifted to MMC2 as shown in Fig. 9 (d) and Fig. 9 (f). Therefore, the power transmission from LCC as presented in Fig. 9 (g) is not affected during AC fault. The DC voltage of MMC1 in Fig. 9 (c) is also maintained close to its nominal value during transient-state. After the fault is cleared, the power of MMC1 is quickly recovered. This test validates that the three-terminal system can operate continuously during the AC fault.

C. DC Fault Ride-through Test

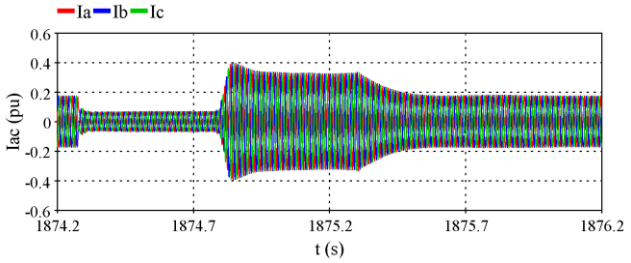
The control strategy of the three-terminal system during normal operation in this section is the same as previous section. A pole to pole DC fault is applied at MMC1 and it lasts for 0.5 s. As presented in Fig. 10 (a), the DC fault is applied at *t*=1874.3 s, the DC bus voltage of MMC1 is dropped to 0. The MMCs operate as STATCOM and supply the reactive power as shown in Fig. 10 (d). As depicted in Fig. 10 (f), the LCC can block the DC fault current by increasing



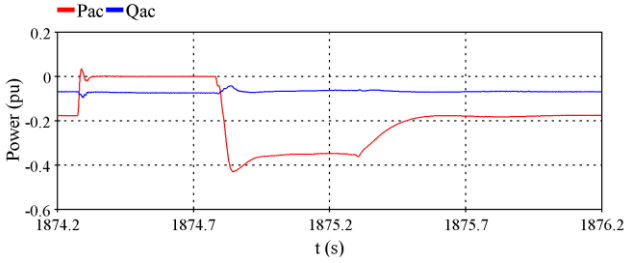
(a) DC voltage of MMC1



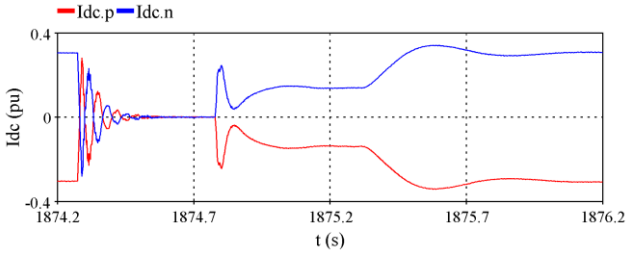
(b) DC current of MMC1



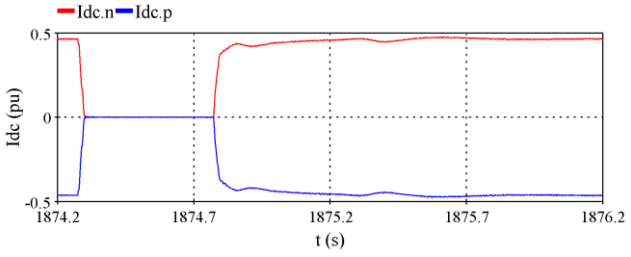
(c) AC current of MMC1



(d) Active and reactive power of MMC1



(e) DC current of MMC2



(f) DC current of LCC

Fig. 10. DC fault ride-through test of the three-terminal hybrid HVDC.

the firing angles to operate at the inverter mode. After the clearance of the DC fault, the three-terminal system is

recovered quickly to normal operation. The DC fault ride-through capability of the system is validated by this test.

V. Conclusions

This paper describes the design principles of an LCC-MMC three-terminal HVDC project planned in south China connecting generation and load center distributed in three provinces. The system configuration with the LCC rectifier at the source side and the hybrid MMC inverter at the two load sides can reduce the system cost and improve the reliability. The hybrid MMC with 70% FBSMs per arm can deliver the power at a reduced DC bus voltage, supply reactive power during AC fault and ride through DC fault. The performance of the LCC-MMC multi-terminal HVDC system in transients and fault conditions is validated through HIL tests with manufacturer's controller replicas on a real-time test bench. The hybrid SMs of the MMC are modelled using an equivalent circuit and implemented in real-time. The HIL results indicate that the LCC-MMC system can operate at reduced dc voltage mode and ride-through AC or DC short-circuit faults.

VI. References

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," IEEE Trans. Power Electron., vol. 24, no. 3, pp. 592–602, Mar. 2009.

[2] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in Proc. IEEE Power Tech Conf., Bologna, Italy, 2003, vol. 3, pp. 23–26.

[3] G. Tang and Z. Xu, "A LCC and MMC hybrid HVDC topology with DC line fault clearance capability," Int. J. Electr. Power Energy Syst., vol. 62, pp. 419–428, 2014.

[4] A. Nami, J. Liang, F. Dijkhuizen and G. D. Demetriades, "Modular multilevel converters for HVDC applications: review on converter cells and functionalities," IEEE Trans. Power Electron., vol. 30, no. 1, pp. 18-36, Jan. 2015.

[5] J. Zhang and C. Zhao, "The research of SM topology with DC fault tolerance in MMC-HVDC," IEEE Trans. Power Del., vol. 30, no. 3, pp. 1561-1568, Jun. 2015.

[6] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barosa, "Operation, control, and applications of the modular multilevel converter: A review," IEEE Trans. Power Electron., vol. 30, no. 1, pp. 37–53, Jan. 2015.

[7] R. Zeng, L. Xu, L. Yao and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," IEEE Trans. Power Electron., vol. 30, no. 3, pp. 1137-1146, Mar. 2015.

[8] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher and B. W. Williams, "Hybrid cascaded modular multilevel converter with DC fault ride-through capability for the HVDC transmission system," IEEE Trans. Power Del., vol. 30, no. 4, pp. 1853-1862, Aug. 2015.

[9] W. Lin, D. Jovcic, S. Nguefeu and H. Saad, "Full-bridge MMC converter optimal design to HVDC operational requirements," IEEE Trans. Power Del., vol. 31, no. 3, pp. 1342-1350, Jun. 2016.

[10] W. Li and J. Bélanger, "An Equivalent Circuit Method for Modelling and Simulation of Modular Multilevel Converters in Real-Time HIL Test Bench," in IEEE Transactions on Power Delivery, vol. 31, no. 5, pp. 2401-2409, Oct. 2016.