Compensation Method for parallel real-time EMT studies

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Abstract—The classical solution for computing electromagnetic transients (EMTs) in parallel relies on the propagation delay of transmission lines. The lines are used as decoupling elements to split the network into different tasks. When there is no natural delay or the delay is too short for the selected simulation time-step, other techniques have to be considered. This paper presents one of them. The compensation method is used in this paper for network decoupling for parallelization. A detailed implementation of this method is presented for real-time simulation. Performances are assessed in both offline and real-time environments with distribution and High Voltage Direct Current (HVDC) network test cases. Switching cases are also studied with HVDC power electronics devices. A Hardware-In-The-Loop (HIL) setup for an HVDC link in operation is also considered to validate the proposed method in a real-time environment.

Keywords: Electromagnetic Transients (EMT), Parallel simulation, Compensation Method, Real-time simulation, Hardware-in-The-Loop.

I. INTRODUCTION

The high penetration of renewable energies has increased the use of power electronics in the transmission network. Transmission Network Operators (TSOs) have to study increasingly complex interaction phenomena between power electronics devices [1]. Also for Distribution Network Operators (DNOs), the development of large active networks can impact the stability of the whole grid [2]. To study the transients of both cases, good accuracy can be achieved by lowering numerical integration time-steps [3] [4] [5]. Parallelization is a key method to accelerate EMT simulation to improve accuracy. It is based on the multi-core properties of modern computers.

One of the main methods to parallelize an EMT simulation relies on the propagation delay of the transmission line model. When, the propagation delay is greater than the time-step, decoupling is possible. This natural latency (line-delay) allows to send computed network values to the next time-step. This method has been implemented for offline and real-time environments. In real-time [6], a topology analysis identifies the transmission lines available for decoupling. Then, it splits the network on each part of the lines and creates tasks. Transmission line-delays are also used in [7], where matrix permutation to block triangular form is applied to establish and solve the decoupled matrices.

When the network model does not contain lines (or cables) with propagation delays, other parallel solution techniques have to be considered. This is the case for large distribution networks [2] or grids with power electronics devices [1].

Attempts to decouple networks when line-delay is not available are typically based on the reformulation of the network matrix into the Bordered Bloc Diagonal (BBD) form. Domain Decomposition techniques [8]-[10] can be used to run the matrix solution in parallel. The main difficulty is that the BBD form may not be optimal for improving computational performance. Also, as explained in [7], existing applications assume linear networks and significant computational performance degradation is expected for nonlinearities and switching topologies due to needed matrix reformulations.

In this paper the compensation method [11] [12] (CM) is used to manually decouple networks at required locations when line-delay decoupling is not available. The CM was initially used for electromagnetic transients when solving nonlinear models [13]. Its extensions and relation with hybridanalysis are discussed in [14]. It can be in fact used for solving separately any number of components in linear and nonlinear mode. The theoretical links between CM, diakoptics and other more recent network tearing approaches are presented in [15]. In fact the original CM is more generic and includes other methods.

To the authors' best knowledge, the CM performances/advantages have not been previously studied for practical problems with switching and real-time simulation.

The paper is organized as follows. The compensation method implementation for EMT offline/real-time environment is presented in Section II. Validation and performance assessments are presented in Section III. for a large distribution network and an industrial HIL application case that includes HVDC converters.

II. COMPENSATION METHOD

A. Overview

The CM uses two main fundamental principles: the Norton/Thévenin equivalents and the superposition theorem. It is equivalent to cutting connecting components, such as wires in a network to create detached subnetworks. It is also possible to cut through branches (linear or nonlinear). The basic principle is illustrated in Fig. 1 using two subnetworks (N_1 and N_2), but it is also applicable to an arbitrary number of subnetworks, assuming that they become independent due to cutting. The cutting connecting components are selected manually.

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Fig. 1. Cutting through wires (dashed line) of two networks using the compensation method.

In summary, the detached subnetworks can be solved in parallel using nodal formulation with discretized component models. This parallel step is followed by the solution of the connecting components and then compensation in N_1 and N_2 for the currents of connecting components. This is illustrated in Fig. 2.



Fig. 2. Ideal current sources to replace the compensation branch

The detailed steps are summarized as follows using Fig. 2. Let us assume n_c cutting (connecting) components. There are two sets of nodes: n_{c1} (size n_c) on the left and n_{c2} (size n_c) on the right. With vector $\mathbf{i_c} = 0$, the networks N_1 and N_2 can be solved in parallel in Step 1 using nodal analysis:

$$Y_1 v_{n1} = i_1$$

 $Y_2 v_{n2} = i_2$ (1)

where Y represents individual admittance matrices, vector v_n holds the unknown nodal voltages and vector i stands for nodal current injections from independent sources and model history terms. The Thevenin voltages v_{th1} and v_{th2} at the node sets n_{c1} and n_{c2} are found directly from the solution of (1) at each simulation time-point.

In Step 2, the Thevenin impedance matrices $(n_c \times n_c)$ are found from (1) using unitary current injections for each *k*th node in sets n_{c1} and n_{c2} , with all independent sources killed:

$$Y_1 v_1 = i_1^{(k)} Y_2 v_2 = i_2^{(k)}$$
(2)

The Thevenin impedances become:

where Z_{th1} and Z_{th2} columns are extracted from corresponding voltages found in v_1 and v_2 of equation (2). These matrices do not change between consecutive time-point solutions if the networks N_1 and N_2 do not encounter topological changes.

In Step 3, it is now possible to compute the branch currents i_{c} using:

$$Z_{C}i_{C} = v_{th2} - v_{th1}$$
(4)
where $Z_{C} = Z_{th1} + Z_{th2} + Z_{B}$. Z_{B} is the connecting

component impedance matrix and it is zero when the connecting components are wires.

In Step 4, the set of currents i_c is used to apply compensation as shown in Fig. 2, using equation (1) and with all independent sources killed. The found final voltage vectors are

$$v_{n1}^{final} = v_{n1} + v_{1C}$$

$$v_{n2}^{final} = v_{n2} + v_{2C}$$
(5)

Where v_{1c} and v_{2c} result from the contributions of i_c .

Steps 1, 2 and 4 can be run in parallel whereas Step-3 is computed sequentially. The classical nodal formulation has been used in this paper in network equation formulation due to initially available setup in [6]. Sparse LU decomposition is used to solve nodal equations.

For switching subnetworks, the compensation impedance matrix is updated and then re-factorized. It occurs each time a Thevenin equivalent impedance changes.

B. Parallelism mechanisms

The above CM is a decoupling method that can be combined with the classical solution based on natural delays of transmission lines. First, the network is split into several sub-networks according to the line-delays. Second, the CM can be applied to the subnetworks. Then, a task is created for each subnetwork for which Steps 1-2-4 are performed in parallel. The compensation task is dedicated to Step 4. The barrier mechanism handles data exchanges between compensation and subnetworks tasks. It is a common mechanism to synchronize threads in parallel. Two barriers are used: one to obtain all Thevenin equivalents (from each subnetwork), and another to broadcast the results of the compensation solution. Fig. 3 illustrates the case of three tasks compensation method with two barriers. It can be reduced to two tasks if the compensation computation is done within a subnetwork task.



Fig. 3. Overview of a three tasks compensation algorithm.

After the splitting process, each task is mapped to a thread: one thread for each subnetwork and one thread for the compensation. The nodal solution and the computation of history currents of subnetworks is done in the same task. Each thread is executed in one simulation core. An automatic task mapping [16] can be run over this first mapping to allocate tasks from control systems or subnetwork split during linedelay analysis.

The compensation split is done manually in this paper. In

most cases, it is a convenient method when the user knows where to cut the simulated for best performance gains. For very large network, it can be automated using the BBD approach, see also [15].

III. VALIDATION AND PERFORMANCE

A. Distribution Network

Very large distribution networks strongly benefit from the compensation decoupling used in this paper, as power lines have propagation delays smaller than the simulation time-step. The test network illustrated in Fig. 4 is a 20kV distribution grid composed of 600 nodes connected to a 63kV grid. It is a benchmark model from [6] with the same complexity as a national distribution grid [2]. Power lines are modeled with R-L impedances. According to EMT studies standard recommendations [3], this simplistic modelling can be used for studies which involve slow control response. It has the downside to slow down the simulation as no line-delays are available for decoupling. Loads are represented by a dynamic load model from [17] using controlled voltage sources. The tearing is feeder-cluster oriented and done manually as illustrated in Fig. 4. The test scenario is a 1s simulation at 50µs time step with a single-phase-to-ground fault of $1m\Omega$ located at the 20kV side of the 63kV/20kV power transformer (Fig. 5). The 100ms fault is initiated at t=0.2s. This test case can be considered as linear: the nodal admittance matrix is refactorized at t=0.2s when the fault is initiated.



Fig. 4. Tasks separation of a 600 nodes 20kV feeder.

Two architectures are used. Arch1 is a laptop computer with Intel i7-6820HQ CPU @ 2.70GH. Arch2 is an OP5031 target 64 bits Linux with 32 cores (2 CPU Intel Xeon E5 3,2 GHz - 16 cores). Arch2 can be run in offline or real-time mode, Arch1 is only for the offline mode. For offline cases, the average realized time-step is measured. For real-time case, only SIL (Software-In-Loop) is run. The minimum time-steps with no overruns are displayed on the last column.

TABLE I PERFORMANCE COMPARISON BETWEEN COMPENSATION AND NORMAL CASE

Test case	Nb Cores	Exec Time Arch1	Exec Time Arch2	RT Time Step	Speed up RT
Normal	1	221 µs	137 µs	145 µs	-
Parallel 1 cuts (comp2)	2	123 μs	67 us	73 µs	1,99
Parallel 3 cuts (comp4)	4	94 µs	38 µs	40 µs	3,63

Currents at the 20kV feeder root (Fig. 6) are compared using the following relative error formula (Fig. 7): $|e_{compensation} - e_{normal}|$



Fig. 5. Three phase voltage at the feeder root during the mono-phase fault (normal case).





Fig. 7 Relative error of the 20kV feeder root current comparison.

It is clear that for large linear distribution grids the compensation method is an efficient solution to parallelize network solution without compromising accuracy (as expected from theory). Only numerical noise is observed in Fig. 7. Additionally, it lowers the acceptable time-step for SIL real-time simulation.

B. HVDC test case

Networks with HVDC devices are another application for the CM as no power lines can be used to split the solution of large power converters. The test case is composed of the HVDC interconnection between France (Les Mandarins) and United Kingdom (Sellindge) called IFA2000 [18] in operation since 1986. It is composed of two LCC bipoles (Line Commutated Converter) of 1000 MW each. The operating voltage is set to +/- 272 kV. For EMT simulation, it can be considered as a switching network as the thyristors commute several times during the simulation. As depicted in Fig. 8, each DC pole is represented by two detailed 6-pulse bridges. Frequency dependent cable models [19] are used to represent the 73km long DC cables. Filters are also modeled in detail. A model of the HVDC control system is imported from Matlab Simulink software using an EMT-Simulink interface [20]. 400kV AC grids are modeled with a source and an impedance representing the short circuit level.

The natural delay of DC cables is used to decouple the solutions of the two converter stations. It results in six tasks with the solution of lines. However, the solution of converter stations is very complex and cannot be split without adding fictitious lines. The CM can be applied here to split each converter station solution in 2 subtasks as shown in Fig. 8. In detail, as network solutions of both converters are independent, two compensation tasks (Fig. 3) are created to compute compensation currents. Those tasks will be done within a substation task, respectively in Proc1 and Proc3.





When CM is not used, four cores are required. When CM is used, the entire system is solved on six cores. Performances of the solution of this system for real-time simulation are compared with a 30µs time step. To illustrate, a 200MW power transfer is set from Les Mandarins (France) to Sellindge (UK). Fig. 9 shows the execution time of the largest task solved for the circuit presented in Fig. 8. The real-time simulation runs on an industrial PC - OP5031 target 32 bits Linux with 32 cores (2 CPU Intel Xeon E5 3,2GHz - 16 cores). A better computational speed is achieved with the CM. Better performance is also noticed when converters are deblocked at 6.3s. The execution time increases when converters are deblocked because refactorization of the admittances matrices are required (thyristors are modeled with 2-value resistors). It avoids overruns observed in the normal case.

In Fig. 10, DC voltages are compared between the normal case and the compensation during the 10s SIL simulation. The first spike is linked to transients from starting the simulation. About 6s, the HDVC interconnection starts and thyristors commute.



Fig. 9. Execution time of the heaviest loaded processor for normal and compensation case SIL real-time simulation of 30 μ s.



Fig. 10. DC voltage for normal and compensation case.



Fig. 11. Relative error of the DC voltage between compensation and the normal case.

Results show that the CM has improved the performance while keeping a good accuracy for a switching network. However, the relative error is higher than in the linear system presented in Section III. A. This comes from several matrix re-factorizations using a constant pivot which increase the numerical errors. Moreover, if the compensation method is used to split further the network (for instance, decoupling the 6-pulse bridges), the simulation is instable. In theory, the compensation allows to cut everywhere in a network. However, application of the compensation method can result in ill-conditioned matrices (see also [14]). This can lead to higher numerical error and in some conditions to instabilities. Different pivoting strategies or scaling in the LU decomposition will be investigated in the next steps of this work to mitigate this issue.

C. HVDC HIL Setup

1) AC fault

The validation in a Hardware-In-The-Loop environment is also done with the IFA2000 HVDC interconnection. Modelling of the electrical system is the same than in previous section. In Fig. 12, the Simulink control system is replaced by the physical control and protection replica described in [18]. Inputs-Outputs (IOs) boards are used to interface the real-time simulator with the control replica. A 40ms single phase to ground fault on the French side is simulated at maximum power transfer (1000 MW) from France to UK. (Fig. 13). A 40µs time step is selected and results are compared with and without compensation. The real-time simulation is run on an OP5031 target 32 bits Linux with 32 cores (2 CPU Intel Xeon E5 3,2GHz - 8 cores). The CM needs 4 cores for the 4 substations whereas 3 cores are required for the normal case. Fig. 12 shows also the task mapping for compensation.



Fig. 12. Overview of the HIL modelling step up and task mapping.

Fig. 14 shows the computed DC voltages with and without compensation. Moreover, the compensation offers better performances in terms of calculation speed with a gain of 40% in comparison with the classical decoupling method (Fig. 15).



Fig. 13. AC voltage at Les Mandarins during one phase-to-ground fault (normal case).



Fig. 14. DC voltage for the one phase-to-ground fault.



Fig. 15. Execution of the heaviest loaded processor for normal and compensation cases.

2) Transformer energization

The same HIL setup is used to analyze the impact of a transformer energization on the French side [21]. To do so, a more detailed model of the French AC grid is used (Fig. 16). Substations close to the IFA2000 converter station are detailed and a Frequency Dependent Network Equivalent (FDNE) [20] is used to represent the rest of the French network. Power transfer is set to 1000MW from UK to France. Energization occurs in a t=3s (Fig. 17). Switching times are respectively for phase A, B, C, t_A =128ms, t_B =129ms, t_c =119ms. This energization leads AC voltage disturbances, commutation on

the French side and finally a permanent trip of the HVDC interconnection (Fig. 17). This test case runs at 40μ s. It requires 5 cores when the classical decoupling method is used. 8 cores are required when the CM is used.



Fig. 16. Overview of substations around Les Mandarins to study transformers energization.

For fast transients, the compensation method gives a similar response (Fig. 18). The shift observed comes from non-synchronize energization events and different replica states between the two simulations. Refactorization numerical errors in III. B. can have an impact too. Before the whole interconnection trip, performances have still improved by 30% (Fig. 19).



Fig. 17. AC currents before a 6-pulse bridge (normal case).



Fig. 18. DC voltage under transformers energization and station trip for normal and compensation cases.



Fig. 19. Execution time of the heaviest loaded processor for normal and compensation cases.

IV. CONCLUSIONS

The compensation method applied in this paper has demonstrated to be an efficient decoupling technique when there are no natural transmission line delays in the simulated system. The compensation method offers quite interesting performances in terms of computational speed while maintaining accuracy. The presented work demonstrates that this method allows to solve switching networks, such as HVDC and large distribution grids. It has been shown that the simulation time-step can be decreased for real-time EMT studies using the compensation method. To the authors best knowledge this is the first time that performances of the compensation method have been tested and documented for practical systems in a real-time environment. Some limitations have been identified. It is not always possible to cut everywhere without avoiding ill-conditioned matrices. Additionally, several re-factorizations can increase the numerical errors. Future works on the linear solver techniques are required to mitigate it.

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