Zero-current Suppression Control for Fault Current Damper based on Model Predictive Control

Ajay Shetgaonkar, Marjan Popov, Peter Palensky and Aleksandra Lekić

***Abstract*—In a multi-terminal direct current (MTdc) system based on a modular multilevel converter (MMC), high-speed and large interruption capability direct current circuit breakers (dc CBs) are required for dc fault interruption. However, the commercialisation of these breakers is challenging, especially offshore, due to the large footprint of the surge arrester. Hence, a supplementary control is required to limit the rate of current rise along with the fault current limiter. Furthermore, the operation of the dc CB is not frequent, thus, it can lead to delays in fault interruption. This study proposes the indirect model predictive control (MPC)-based zero-current control. This control provides dc fault current suppression by continuously controlling the zero-sequence current component using circulating current suppression control (CCSC), and by providing feedback to the outer voltage loop and inner current loop of MMCs. The proposed control is simulated for pole-to-pole and pole-to-ground faults at the critical fault location of an MTdc system. The simulation is performed in Real Time Digital Simulator (RTDS) environment, which shows that the predictive control reduces the rate of rise of the fault current, and in this way provides an additional 3 ms after the dc fault occurrence for the dc CB to clear the fault. Besides, the energy absorbed by the dc CB's surge arrester during the pole-to-pole and pole-to-ground fault remains the same with the proposed control.**

***Keywords*—Multiterminal HVDC grids, RTDS, Model Predictive Control, dc circuit breakers**

I. Introduction

HIGH power direct current transmission grid with a meshed modular multilevel (MMC) converter is considered as a promising technology for extensive offshore wind power integration in Europe [1]. The Europe's expected new wind farm capacity of 116 GW during 2022-2026 [2]. Based on submodules' (SMs) design and configuration, the MMC technology is classified into half-bridge (HB), full-bridge (FB) and Hybrid MMC [3]. However, HB-MMCs are commissioned due to their lower footprint and cost. This comes up with another drawback: the lack of direct current (dc) fault interruption capability. During a fault period, unlike ac systems, dc systems does not have a natural current zero crossing, and therefore, a direct current circuit breaker (dc CB) is needed. In the last decade, different dc CBs have been proposed, prototyped and tested for the application in the MTdc systems [4], [5], [6]. The dc fault interruption in HB-MMC-based MTdc systems has to be ultra-fast (< 3 ms) due to the high rate of rise of the dc current. In practice, to limit the fault current, the Fault Current Limiters, in the form of rectors, are added, and used for dc fault detection [7]. However, the high value of the inductance (> 150 mH) impacts the controllability of converters and increases the capital cost of the dc grid [8]. Another method to control the fault current, is to regulate the pole-to-pole voltage near the converter, which is known as a Fault Current Suppression (FSC) method. In [9], [10], a combination of hybrid-MMC and droop control is applied, which regulates the arm voltage as a way to decrease the fault current. A similar concept for a HB-MMC is used in [11], [12]. Furthermore, the authors also compared different methods of FSC. Similarly, [13] provides a soft current suppression control in the outer voltage loop. In [14] a notch filter is applied to extract the dc component and to regulate the fault current only during the fault occurrence. The suppression methods mentioned earlier imply proportional-integral (PI)-based control action, either in the outer voltage loop or by using a circulating current suppression control (CCSC). In [15], a suppression control was proposed for the FB-MMC MTdc using CSCC together with a protection scheme. These controls are based on a mode selection during the fault; thus, the stability of these controls is undetermined [16]. The fault interruption creates a temporary instability in the dc grid, and is propagated into ac systems where renewable energy resources are connected, which are more susceptible to disturbances. Hence, the post-fault clearance is crucial. In the existing literature dealing with suppression control, MTdc systems are simplified with respect to the offshore grid, and its control with respect to the offline simulation. Thus, the dynamics of the offshore grid is removed. The existing suppression controls are implemented with PI, which introduces inherent slower performance limitations [17], [18].

In the CCSC, a zero-sequence current component of dqz-frame current representation can be viewed as one third of the dc current (i_{dc}). However, this current, in the traditional strategies, is either left uncontrolled [19] or is employed in energy control [20]. In this paper, we propose a controller to the mentioned zero-current, to decrease the fault amplitude and to smooth the fault recovery. Furthermore, the model predictive control (MPC) has proven its superiority over conventional PI control in controlling complex non-linear, multiple-input multiple-output (MIMO) systems in different industrial sectors [21].

This paper introduces the indirect MPC-based zero-current control employed for dc fault current suppression. The CCSC provides a reference to the Outer Voltage Control and Direct Voltage Control. The proposed suppression control provides control during a dc fault, which regulates the fault current amplitude by reducing the rate of rise of the fault current. As

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a result, it provides an extra time margin for fault detection or dc CB breaker operation without affecting the circulating current suppression in the MMC arm. Additionally, the better post-fault recovery is achieved. The proposed control can also be added to the existing traditional PI control without creating system instability due to quadratic cost function formulation. Furthermore, the performance of CCSC is tested under different faults in the real-time digital simulator (RTDS) with the detailed equivalent models of the offshore wind farm, HB-MMC, and dc CBs.

In Section II, the configuration of the MMC and the existing controls are analyzed. The proposed indirect MPC-based method is described in Section III. The MTdc setup and the simulation results are elaborated in Section IV. Finally, meaningful conclusions are presented in Section V.

II. MMC Model and Control

A decade of development in modelling of MMCs has led to an accurate MMC non-linear model [18]. The dynamics of the MMC can be formulated by using two components, Σ and Δ, which represent the dc and ac characteristics of the converter respectively. By applying the Clarke-park transformation, the Σ and Δ ac components are translated into the stationary $dq-$frame:

$$\frac{d}{dt}\left(\vec{i}_{dq}^{\Delta}\right) = \frac{\vec{v}_{Mdq}^{\Delta} - \left(\omega L_{eq}^{ac} J_2 + R_{eq}^{ac} I_2\right)\vec{i}_{dq}^{\Delta} \; - \; \vec{v}_{dq}^{G}}{L_{eq}^{ac}}, \quad \text{(1a)}$$

$$\frac{d}{dt}\left(\vec{i}_{dq}^{\Sigma}\right) = -\frac{\vec{v}_{Mdq}^{\Sigma} \; + \; \left(R_{arm} I_2 - 2\omega L_{arm} J_2\right)\vec{i}_{dq}^{\Sigma}}{L_{arm}}, \quad \text{(1b)}$$

$$\frac{d}{dt}\left(i_{z}^{\Sigma}\right) = \; \frac{v_{dc}}{2L_{arm}} - \frac{v_{Mz}^{\Sigma} + R_{arm} \; i_{z}^{\Sigma}}{L_{arm}}, \quad \text{(1c)}$$

where $L_{eq}^{ac} = L_r + \frac{L_{arm}}{2}$, $R_{eq}^{ac} = R_r + \frac{R_{arm}}{2}$, $J_2 = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$, $I_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$, and

$$i_{d,q}^{\Delta} = i_{d,q}^{U} - i_{d,q}^{L}, \quad i_{d,q,z}^{\Sigma} = \frac{i_{d,q,z}^{U} + i_{d,q,z}^{L}}{2},$$
$$v_{Md,q}^{\Delta} = \frac{-v_{Md,q}^{U} + v_{Md,q}^{L}}{2}, \quad v_{Md,q,z}^{\Sigma} = \frac{v_{Md,q,z}^{U} + v_{Md,q,z}^{L}}{2}.$$

A. MMC control design

In the MTdc, each onshore converter consists of three primary control loops [22], namely, Outer Voltage Control (OVC), Inner current control (ICC) and Circulating Current Suppression control(CCSC), as shown in Fig. 1. Fig. 2 highlights the PI controls of the onshore and the offshore converters. The OVC provides references to the ICC. The setpoints to the OVC are provided by the *Dispatch level* via TCP/IP communication interface, as it is shown in Fig. 1. The setpoint signals include dc voltage $V_{dc,ref}$, ac voltage $V_{ac,ref}$, active $P_{ac,ref}$ and reactive $Q_{ac,ref}$ power, and frequency f. The selection of these signals depends upon the control mode (i.e. constant DC voltage, Grid forming, Active-Reactive power control-mode). Dispatch controls are typically operated by the system operators. The system operators, provide the setpoint based on the power ac/dc power flow and day-ahead demand.

The ICC loop generates the modulating voltages ($v_{M,dq}^{\Delta}$) based on the feedforward terms ($v_{g,dq}^{\Delta}$ and v_{dc}). The ICC and OVC are only responsible for the fundamental and the odd-harmonic components of the grid current. The CSCC controls the DC and even harmonic components of the grid current. The presence of the even harmonic results in the losses within the converter. Hence, these currents are suppressed by generating modulated voltage ($v_{M,dq}^{\Sigma}$), and as a result, only the DC component is present.

The offshore converter consists of DVC and CCSC. The DVC is the simplest form of grid-forming control [22]. Similar, to onshore converters, the offshore converter receives setpoint commands from the dispatch control. The modulating voltages ($v_{M,dq}^{\Delta,\Sigma}$) are converted into a firing sequence. Traditionally, these controls are implemented using the PI controller by transforming ac measurements from the abc-frame into the stationary dq-frame by making use of a phase lock loop (PLL) except grid forming control, which uses an oscillator [19]. The control system of the type-4 wind turbines is the same as reported in [17].

III. MPC-Based Zero-Current Control

As the name indicates, the prediction and the accuracy of the MPC are purely determined by the system behaviour. The dq-frame mathematical model of the MMC is represented by equations (1), and is rewritten in a matrix discrete form as:

$$\begin{bmatrix} \Delta\vec{x}(k+1) \\ \vec{y}(k+1) \end{bmatrix} = \overbrace{\begin{bmatrix} \mathbf{F}(T_s) & o^T \\ \mathbf{H}(T_s)\mathbf{F}(T_s) & 1 \end{bmatrix}}^{A_d} \overbrace{\begin{bmatrix} \Delta\vec{x}(k) \\ \vec{y}(k) \end{bmatrix}}^{\vec{x}_m(k)} \quad \text{(3a)}$$

$$+ \overbrace{\begin{bmatrix} \mathbf{G}(T_s) \\ \mathbf{H}(T_s)\mathbf{G}(T_s) \end{bmatrix}}^{B_d} \Delta\vec{u}(k), \quad \text{(3b)}$$

$$\vec{y}_m(k) = \overbrace{\begin{bmatrix} 0 & \mathbf{I} \end{bmatrix}}^{C_d} \vec{x}_m(k), \quad \text{(3c)}$$

where $k \in \mathbb{N}$ indicates discrete time step, $\mathbf{H}(T_s)$ is an identity matrix, whereas $\mathbf{F}(T_s) = e^{\mathbf{A}\,T_s}$ and $\mathbf{G}(T_s) = \mathbf{A}^{-1}\left(e^{\mathbf{A}\,T_s} - \mathbf{I}\right)\mathbf{B}$. Matrices $\mathbf{A}$ and $\mathbf{B}$ are defined as

$$\mathbf{A} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & 2\omega & 0 & 0 & 0 \\ -2\omega & -\frac{R_{arm}}{L_{arm}} & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{arm}}{L_{arm}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_{eq}^{ac}}{L_{eq}^{ac}} & -\omega \\ 0 & 0 & 0 & \omega & -\frac{R_{eq}^{ac}}{L_{eq}^{ac}} \end{bmatrix}, \quad \text{(4a)}$$

$$\mathbf{B} = \text{diag}\left\{-\frac{1}{L_{arm}}, -\frac{1}{L_{arm}}, -\frac{1}{L_{arm}}, \frac{1}{L_{eq}^{ac}}, \frac{1}{L_{eq}^{ac}}\right\}, \quad \text{(4b)}$$

with $T_s \in \mathbb{R}$ as the sampling time, with value $T_s = 40\,\mu$s. Furthermore, the augmented state is defined as $\Delta\vec{x}(k) = \vec{x}(k) - \vec{x}(k-1)$, where $\vec{x}(k) \in \mathbb{R}^5$ indicates the system state vector at k^{th} instant and $\vec{x}(k-1)$ indicates vector of states for the previous sampling instance $k-1$. Similarly, the augmented input is defined as $\Delta\vec{u}(k) = \vec{u}(k) - \vec{u}(k-1)$, where $\vec{u}(k)$ represent the system inputs at k^{th} instant and $\vec{u}(k-1)$ indicates the past inputs.

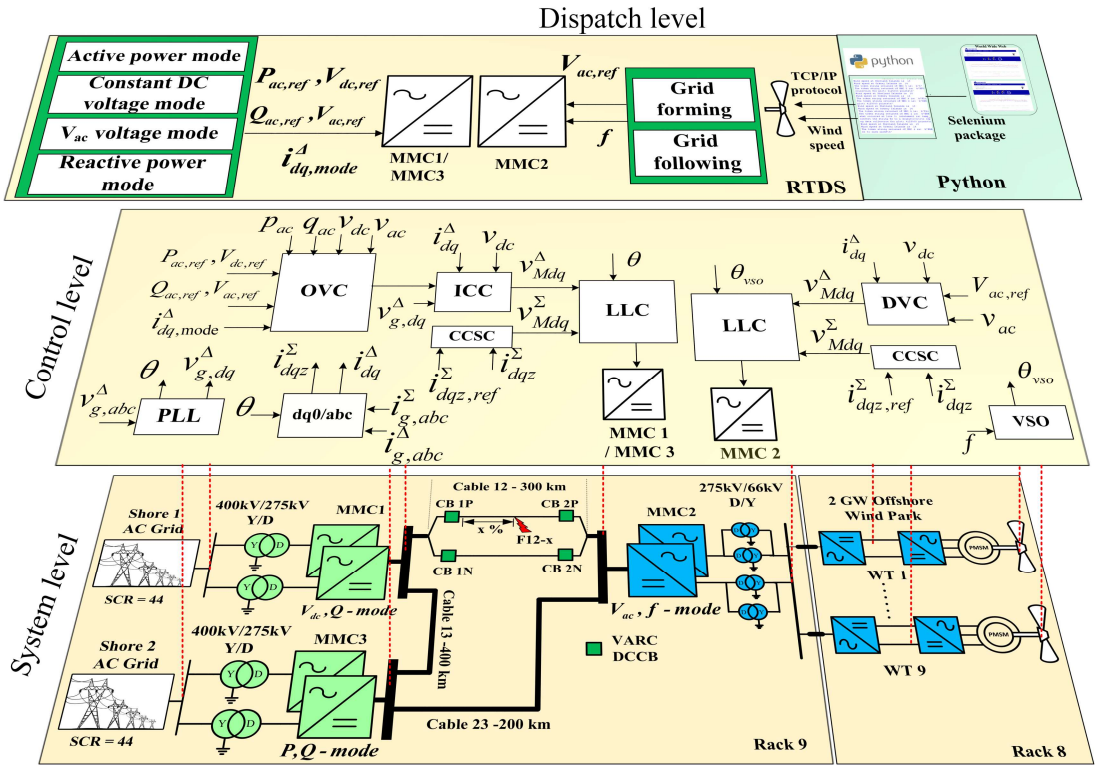

Fig. 1. Circuit and control hierarchy of Three terminal ±525 kV bipolar Mtdc simulated systems (The red dotted line indicates the ac-dc measurement).

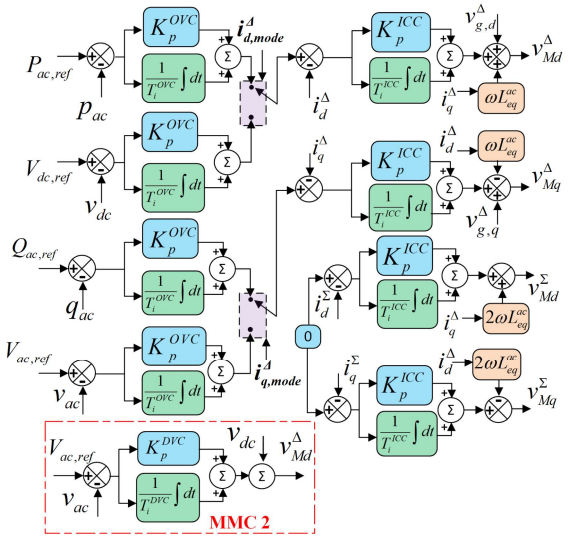

Fig. 2. The traditional PI-based MMC control design.

The vector $\vec{x} = [i^{\Sigma}_{d},\ i^{\Sigma}_{q},\ i^{\Sigma}_{z},\ i^{\Delta}_{d},\ i^{\Delta}_{q}]^{T}$ represents state variables, while $\vec{u} = [v^{\Sigma}_{Md},\ v^{\Sigma}_{Mq},\ v^{\Sigma}_{Mz} - \frac{v_{dc}}{2},\ v_{Md} - v^{\Delta}_{d},\ v_{Mq} - v^{\Delta}_{q}]^{T}$, $\vec{u} \in \mathbb{U} = [-1, 1]^5 \subset \mathbb{R}$, represents system inputs. Similarly to [17], the future control sequence is represented by the discrete Laguerre network, $\vec{\eta} \in [-1, 1]^5 \subset \mathbb{R}$, which is determined by solving the optimal control problem, and minimizing the objective (cost) function, subjected to the equality and inequality constraints:

$$\min_{\vec{\eta}} \ J = \sum_{i=1}^{N_p} \|\vec{x}_m(k+i|k)\|^2_{\mathbf{Q}} + \|\vec{\eta}\|^2_{\mathbf{R}} + I_m e(k), \qquad (5a)$$

$$\text{subject to } \mathbf{M}\vec{\eta} \leq \vec{b}, \qquad (5b)$$

$$\vec{x}_m(k+i|k) = \vec{r}(k) - \vec{y}_m(k|k). \qquad (5c)$$

Here, $\mathbf{Q} \succeq 0$ and $\mathbf{R} \succ 0$ are weighting matrices, and $N_p = 20 \in \mathbb{I}^{+}$ is the prediction horizon. For variables $\vec{x}_m(k)$, vector $r(k) \in \mathbb{R}^5$ is a reference signal. The Matrix $\mathbf{M}$ and the column vector $\vec{b}$ are related to the constraint information of the rate and amplitude [17]. In reality, there will be an error due to the modelling or the signal noise. However, these disturbances can be considered in the optimal control problem, which is represented by $e(k)$. With $e(k)$ is denoted the error between the system's measured signal and the plant's predicted signal at k^{th} instance. $I_m \succ 0$ is the weight matrix. The

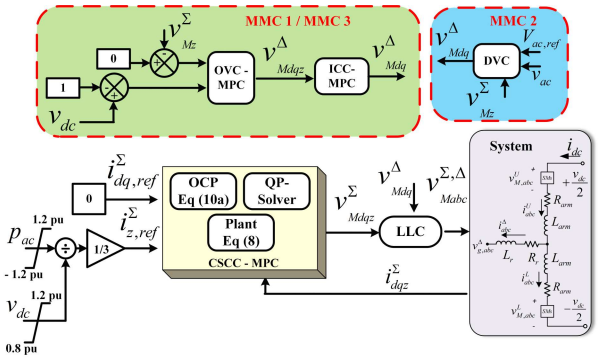

Fig. 3. Block diagram of implemented zero-current control.

reference determination of the differential-current components (denoted as $i^{\Delta}_{d,q}$) remains the same as of the traditional control hierarchy as explained in the section II.A. The CCSC mainly suppresses additive currents in the traditional control. However, the zero-current component (i^{Σ}_{z}) reference is left uncontrolled. The previous section explains that the MMC current on dc side can be represent by zero current component. In this paper, zero-current reference is calculated by using the

active power injected/absorbed in the ac system and the dc voltage as shown in Fig. 3.

During the stable operation, the active power and the dc voltages are inside the prescribed limits (i.e. ± 1.2 p.u, and 1 p.u $-$ 0.8 p.u, respectively). Hence, the calculated zero-current component remains the same as the measured one. During the dc fault period, the active power P_{ac} increases and the dc voltage v_{dc} decreases, which leads to saturation of the calculated current. In order to reduce the fault current, the voltage at the MMC terminals is reduced, which results in a decrease in the rate of rise of the fault current across the line inductance (l_{line}). Hence, the zero-current controller provides the control action which temporally reduces the DC link voltage and lowers the fault current. Also, this control action is added to the outer voltage loop and direct voltage control in the case of grid forming converters (as shown in Fig. 3), to ensure that both ac and dc component values remain within the operating limits.

IV. Experimental Studies

For the purpose of demonstration of the proposed control advantages, the state-of-the-art model for the ± 525 kV, 2 GW dc terminals is designed and simulated. Fig. 1 shows the simulated three terminal ± 525 kV ground return bipolar MTdc system programmed for the real-time simulation in the RSCAD/RTDS. The system is divided into two zones (i.e., onshore and offshore). The onshore system consists of two converters (i.e. MMC1 and MMC3). Each platform is connected to two 1 GW MMC converters. The onshore platforms are connected to a strong grid, with a short circuit ratio of $SCR = 44$, by two converter transformers with a rating of $400/275$ kV, 1250 MVA. Similarly, the offshore platform has two 1 GW MMC converters connected to a wind farm via $275/66$ kV, 1250 MVA. This transformer also acts as a scaling transformer. The offshore platform is connected to the wind park by a 66 kV ac cable with a distance of 7 km. The ground for the MTdc is provided at the onshore platform with the resistance value of $0.01\,\Omega$. The onshore zone is connected to the offshore zone by three 2 GW, 525 kV HVDC cables with the ratings given in Fig. 1. Cable 12 has two VSC-assisted resonant current (VARC) dc circuit breakers (CBs) at each cable's end. This VARC dc CB is scaled to 525 kV with a fault interruption capability of 20 kA [5]. The wind park has nine Type-4 wind turbines, each with a rating of 2 MW at 16 m/s. The wind speed data is updated in real-time through a North Sea sensor using a python script [17].

Table I highlights the circuit parameters for the converters given in Fig. 1. The proposed controls are located in both offshore and onshore converters. The onshore grid-tie converter station, MMC1 controls dc voltage (V_{dc}, Q-mode), whilst MMC3 controls active power (P, Q-mode). The offshore converter MMC2 is grid forming converter (v_{ac}, f-mode).

In a steady-state, MMC2 injects an active power of 2 GW into the dc grid generated by the wind power plant. MMC3 injects an active power of 1 GW into the onshore ac grid. In order to keep the dc-link voltage constant, the remaining power is absorbed by MMC1, and injected into the onshore ac grid.

TABLE I
Circuit Parameter for the Simulated System

Parameter		Values
Rated capacity		2000 MVA
Control Mode	MMC1	V_{dc}, Q
	MMC2	V_{ac}, Q
	MMC3	P, Q
DC link voltage (v_{dc})		$\pm$ 525 kV
Number of Submodules per arm (N_{sm})		240
Arm capacitance (C_{arm})		22 μF
Arm inductance (L_{arm})		42 mH
Arm resistance (R_{arm})		0.544 Ω
Transformer leakage reactance (l_r)		0.18 p.u
AC converter voltage (onshore)		275 kV
AC system voltage (onshore/offshore)		400 kV/66 kV
DC line inductance(l_{line})		120 mH
AC frequency(f)		50 Hz

Due to a full selective protection scheme being introduced [5], the internal protection of converters is disabled. The rated fault current interruption capability of the VARC dc CB is set to 20 kA, and the operating time of the dc CB is 5 ms. Furthermore, the dc fault detection is not instantaneous, so a delay of 1 ms is introduced.

A. Fault Amplitude identification

In order to identify the current hotspot in the MTdc during the fault, two different types of faults at two different cable locations are simulated. For this work, a positive pole-to-ground (PG) dc fault, and a positive pole-to-negative pole (PP) dc fault are selected. These faults are located at the MMC1's terminal (0 %) and near the opposite terminal (100 %). The nomenclature; $PG-0-12$ in Fig.4 indicates the PG dc fault at the terminal in cable 12. Similarly, $PG-100-12$ indicates the PG dc fault at the opposite terminal of cable 12. Furthermore, I^{+}_{linexy} indicates the current measured in the cable xy from x terminal of the cable.

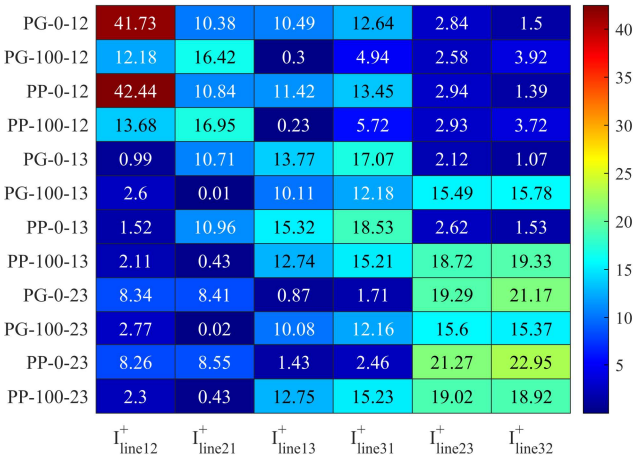

Fig. 4. Fault amplitude in kA at 6 ms for different fault types and locations in MTdc.

Fig. 4 indicates the fault current measured at $t = 6$ ms without any fault current limiting scenario at different locations during different faults. The analysis shows that, for a given MTdc system at rated power, the PG and the PP fault near the MMC1 create fault currents with amplitudes 41.73 kA and 42.44 kA, respectively. Similarly, the fault near MMC2, on cable 23 produces the second highest fault current.

The converters' pre-fault condition and the operating mode determine the fault current amplitude. Since MMC1 regulates the dc link voltage to a constant value, the fault near this terminal results in a high fault current. Similarly, the fault near MMC2 produces a high fault current due to the ac power infeed. Hence, the next study considers the fault near MMC1 and MMC2 on cable 12.

To understand the impact of the proposed control strategies, the following cases are investigated:

C1 Traditional PI control without zero-current control.
C2 MPC control without zero-current control.
C3 Traditional PI control with zero-current control.
C4 MPC control with zero-current control.

B. DC fault at MMC1's terminal

In this scenario, the PG and PP faults are applied at the terminal of MMC1. Furthermore, the impact of protection delay (i.e delay in fault detection or dc cb operation) (t_d) is investigated for all cases and summarised in Table II and III. From these tables it can be seen that the fault is interrupted by the dc cb with both traditional PI controls, and MPC with a delay of 1 ms. During PG fault with MPC, the peak fault current in CB1P dc CB and MMC1 is lower by 0.7 kA and 1.26 kA, respectively. These lower values result from the MPC's fast control action on the changes of MMC's state variables. However, this action results in an undershoot of 16% in $v_{dc,MMC1}$ voltage. Furthermore, the settling time is increased by 50 ms. The fast action helps the dc CB to absorb less energy. As the delay increases, the peak amplitude of the fault current increases, and as a result, PI controlled system fails to operate. However, the MPC during the PG fault only adds up a surplus 0.5 ms of delay before the dc CB fails to interrupt the fault. A similar trend is observed with a higher fault current and undershoot during the PP fault as shown in Table III.

With the proposed control over i_z^{Σ} current, in PI's and MPC's CCSC, the sensitivity of the t_d is minimised to a greater extent. The system can withstand a higher delay, with a lower fault current in the converter and in the dc CB. This results in a lower energy absorption in the dc CB's surge arrester. The energy absorbed by the traditional PI-controlled MMC is 30% (PG) and 40% (PP) higher than that of the MPC-controlled MMC with the proposed control over i_z^{Σ} current for $t_d = 3$ ms during the PG and the PP fault, respectively. Furthermore, the settling time is shortened due to the active power feedback in the proposed control. However, the impact of these improvements is observed on the undershoot in $v_{dc,MMC1}$. It is also interesting to observe that the energy absorbed during the PG and PP fault interruption remains the same, indicating a reduced effect on Surge arrester during the PP fault. Furthermore, the delay does not increase the absorbed energy drastically.

Fig. 5 highlights the significance of the proposed control compared to the PI and MPC in the time domain. During the fault period, the MMC with the proposed control has $\frac{\mathrm{d}v}{\mathrm{d}t}$ of -114 kV/ms, while PI and MPC controlled MMC has $\frac{\mathrm{d}v_{dc,MMC1}}{\mathrm{d}t}$ of -40 kV/ms. The high value of $\frac{\mathrm{d}v_{dc,MMC1}}{\mathrm{d}t}$ creates reduction in $\frac{\mathrm{d}i_{dc,CB1P}}{\mathrm{d}t}$ of fault current as seen Fig. 5(b). Furthermore, the proposed control prevents a large drop in converters' energy. Hence, it protects the sub-modules during fast transients. The arm currents of the converts are smaller compared to traditional PI-controlled MMC, as seen in Fig. 5(d).

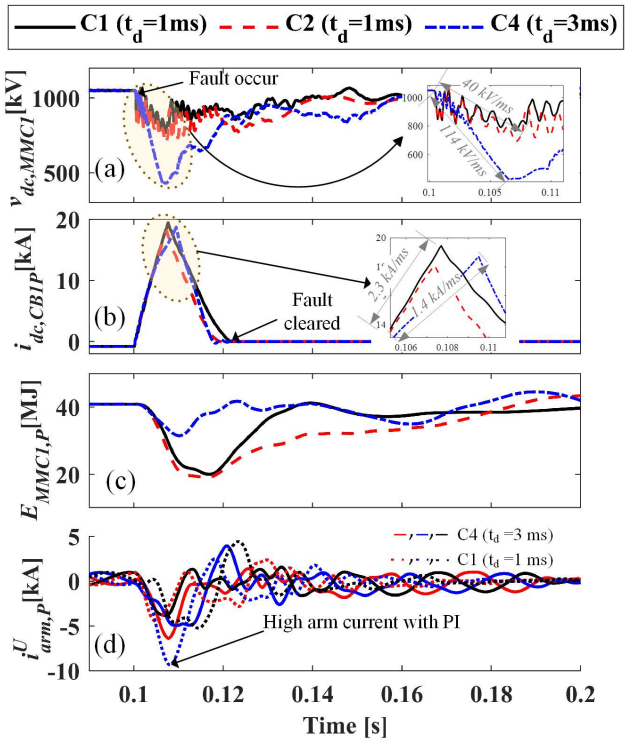

Fig. 5. Impact of proposed control during PP fault at MMC1 terminal: (a) MMC1's terminal voltage [kV]; (b) Line Current [kA] in CB1P dc CB; (c) Total Energy stored in the MMC1 [MJ]; and (d) Upper arm current of MMC1 [kA].

C. DC fault at MMC2 terminal

In this case, a PG and a PP fault is applied at MMC2 terminal. The effect of protection delay is investigated for all cases, and are summarised in Table V and IV, respectively. The DC fault near MMC2 creates a high rate of rise of fault current, which results in current interruption failure. The high value of $\frac{\mathrm{d}v_{dc,MMC2}}{\mathrm{d}t}$ is caused by the wind park's power infeed. Hence, MMC2 is very sensitive to the delay of the operation of dc CB, and the line inductance (l_{line}). However, with the application of the proposed zero-current PI and MPC control, the delay sensitivity is removed for both types of faults as illustrated in Table V and IV for PP and PG faults. The energy absorption and the peak fault current through CB2P and MMC2 for both controls differ by less than 1%. This is caused by the constant current source behaviour of the grid-forming converters. Moreover, on average, the settling time is improved by 100 ms in the case of MPC controlled system. Furthermore, the undershoot percentage during the PP fault is higher compared to that during the PG fault.

V. Conclusion

In this paper, a new MPC zero-current control for the MMC converter is proposed, which influences the dc link voltage control. The proposed control method controls the additive zero current component, and it can provide an extra window of 3 ms for the fault detection or dc CB operation. This control is especially beneficial for a converter that directly influences

TABLE II

PERFORMANCE DIFFERENT CASES UNDER THE POLE-TO-GROUND FAULT AT MMC1 TERMINAL.

pole-to-ground fault		Peak in $i_{dc,CB1P}$	Peak in $i_{dc,MMC1}$	Undershoot in V_{dc}	settling time of V_{dc}	Energy SA	Status
PI without i_z^{Σ} control	$t_d = 1ms$	17.70 kA	15.30 kA	916.31 kV (-12.73 %)	0.13 s	69.25 MJ	**Interrupts**
	$t_d = 1.5ms$	37.01 kA	24.36 kA	533.87 kV (-49.15 %)	Inf	0.00 MJ	**Fails**
	$t_d = 2ms$	36.93 kA	24.46 kA	534.68 kV (-49.07%)	Inf	0.00 MJ	**Fails**
	$t_d = 2.5ms$	36.84 kA	24.51 kA	532.94 kV (-49.24 %)	Inf	0.00 MJ	**Fails**
	$t_d = 3ms$	36.78 kA	24.57 kA	533.79 kV (-49.16 %)	Inf	0.00 MJ	**Fails**
MPC without i_z^{Σ} control	$t_d = 1ms$	17.00 kA	14.04 kA	881.92 kV (-16.00 %)	0.18 s	55.38 MJ	**Interrupts**
	$t_d = 1.5ms$	18.77 kA	15.18 kA	867.75 kV (-17.35 %)	0.19 s	62.27 MJ	**Interrupts**
	$t_d = 2ms$	32.63 kA	22.14 kA	538.90 kV(-48.67 %)	Inf	0.00 MJ	**Fails**
	$t_d = 2.5ms$	32.55 kA	22.18 kA	539.94 kV (-48.57 %)	Inf	0.00 MJ	**Fails**
	$t_d = 3ms$	32.47 kA	22.14 kA	540.47 kV (-48.52 %)	Inf	0.00 MJ	**Fails**
PI with i_z^{Σ} control	$t_d = 1ms$	15.59 kA	11.52 kA	789.86 (-24.78%)	0.18 s	42.5 MJ	**Interrupts**
	$t_d = 1.5ms$	16.53 kA	12.49 kA	790.77 (-24.69%)	0.18 s	47.96 MJ	**Interrupts**
	$t_d = 2ms$	17.57 kA	13.36 kA	789.43 (-24.82%)	0.29 s	53.51 MJ	**Interrupts**
	$t_d = 2.5ms$	18.8 kA	13.88 kA	790.13 (-24.75%)	0.29 s	59.83 MJ	**Interrupts**
	$t_d = 3ms$	47.1 kA	29.51 kA	517.49 (-50.72%)	Inf	0 MJ	**Fails**
MPC with i_z^{Σ} control	$t_d = 1ms$	15.03 kA	9.5 kA	739.02 (-29.62%)	0.16 s	32.33 MJ	**Interrupts**
	$t_d = 1.5ms$	15.76 kA	10.71 kA	739.51 (-29.57%)	0.17 s	36.55 MJ	**Interrupts**
	$t_d = 2ms$	16.5 kA	11.5 kA	738.56 (-29.66%)	0.17 s	40.4 MJ	**Interrupts**
	$t_d = 2.5ms$	17.34 kA	11.95 kA	736.82 (-29.83%)	0.16 s	44.05 MJ	**Interrupts**
	$t_d = 3ms$	18.53 kA	12.53 kA	735.28 (-29.97%)	0.16 s	48.78 MJ	**Interrupts**

TABLE III

PERFORMANCE DIFFERENT CASES UNDER THE POLE-TO-POLE FAULT AT MMC1 TERMINAL.

pole-to-pole fault		Peak in $i_{dc,CB1P}$	Peak in $i_{dc,MMC1}$	Undershoot in V_{dc}	settling time of V_{dc}	Energy SA	Status
PI without i_z^{Σ} control	$t_d = 1ms$	19.46 kA	16.4 kA	767.07 kV (-26.95 %)	0.19 s	84.32 MJ	**Interrupts**
	$t_d = 1.5ms$	43.24 kA	24.94 kA	-14.22 kV (-101.35 %)	Inf	0 MJ	**Fails**
	$t_d = 2ms$	43.16 kA	25.13 kA	-13.62 kV (-101.3 %)	Inf	0 MJ	**Fails**
	$t_d = 2.5ms$	43.08 kA	25.18 kA	-13.88 kV (-101.32 %)	Inf	0 MJ	**Fails**
	$t_d = 3ms$	43 kA	25.25 kA	-13.98 kV (-101.33 %)	Inf	0 MJ	**Fails**
MPC without i_z^{Σ} control	$t_d = 1ms$	18.06 kA	14.7 kA	691.54 kV(-34.14 %)	0.19 s	63.95 MJ	**Interrupts**
	$t_d = 1.5ms$	37.88 kA	22.69 kA	-10.72 kV(-101.02 %)	Inf	0 MJ	**Fails**
	$t_d = 2ms$	37.67 kA	22.76 kA	-15.06 kV(-101.43 %)	Inf	0 MJ	**Fails**
	$t_d = 2.5ms$	37.57 kA	22.79 kA	-14.02 kV(-101.34 %)	Inf	0 MJ	**Fails**
	$t_d = 3ms$	37.44 kA	22.87 kA	-13.36 kV(-101.27 %)	Inf	0 MJ	**Fails**
PI with i_z^{Σ} control	$t_d = 1ms$	15.71 kA	11.34 kA	535.32 kV (-49.02%)	0.25 s	44.57 MJ	**Interrupts**
	$t_d = 1.5ms$	16.63 kA	12.4 kA	530.33 kV (-49.49%)	0.26 s	50.27 MJ	**Interrupts**
	$t_d = 2ms$	17.71 kA	13.12 kA	520 kV (-50.48%)	0.27 s	56.11 MJ	**Interrupts**
	$t_d = 2.5ms$	19.13 kA	13.61 kA	535.75 kV (-48.98%)	0.26 s	64.22 MJ	**Interrupts**
	$t_d = 3ms$	49.91 kA	28.1 kA	-16.5 kV (-101.57%)	Inf	0 MJ	**Fails**
MPC with i_z^{Σ} control	$t_d = 1ms$	15.15 kA	9.27 kA	417.64 kV (-60.22%)	0.18 s	33.31 MJ	**Interrupts**
	$t_d = 1.5ms$	15.87 kA	10.49 kA	418.39 kV (-60.15%)	0.18 s	37.55 MJ	**Interrupts**
	$t_d = 2ms$	16.65 kA	11.36 kA	418.08 kV (-60.18%)	0.18 s	41.61 MJ	**Interrupts**
	$t_d = 2.5ms$	17.52 kA	11.87 kA	422.06 kV (-59.8%)	0.18 s	45.39 MJ	**Interrupts**
	$t_d = 3ms$	18.71 kA	12.21 kA	421.38 kV (-59.87%)	0.17 s	50.34 MJ	**Interrupts**

TABLE IV

PERFORMANCE DIFFERENT CASES UNDER THE POLE-TO-GROUND FAULT AT MMC2 TERMINAL.

pole-to-ground fault		Peak in $i_{dc,CB1P}$	Peak in $i_{dc,MMC2}$	Undershoot in (V_{dc})	settling time (V_{dc})	Energy SA	Status
PI without i_z^{Σ} control	$t_d = 1ms$	36.33 kA	14.77 kA	572.04 kV(-45.52%)	Inf	0 MJ	**Fails**
	$t_d = 1.5ms$	36.41 kA	14.46 kA	568.81 kV(-45.83%)	Inf	0 MJ	**Fails**
	$t_d = 2ms$	36.36 kA	14.49 kA	570.08 kV(-45.71%)	Inf	0 MJ	**Fails**
	$t_d = 2.5ms$	36.37 kA	14.43 kA	568.81 kV(-45.83%)	Inf	0 MJ	**Fails**
	$t_d = 3ms$	36.4 kA	14.43 kA	569.14 kV(-45.8%)	Inf	0 MJ	**Fails**
MPC without i_z^{Σ} control	$t_d = 1ms$	30.12 kA	15.97 kA	606.88 kV(-42.2%)	Inf	0 MJ	**Fails**
	$t_d = 1.5ms$	29.99 kA	15.74 kA	605.47 kV(-42.34%)	Inf	0 MJ	**Fails**
	$t_d = 2ms$	29.85 kA	15.49 kA	604.13 kV(-42.46%)	Inf	0 MJ	**Fails**
	$t_d = 2.5ms$	29.84 kA	15.1 kA	607.27 kV(-42.16%)	Inf	0 MJ	**Fails**
	$t_d = 3ms$	29.75 kA	14.85 kA	605.14 kV(-42.37%)	Inf	0 MJ	**Fails**
PI with i_z^{Σ} control	$t_d = 1ms$	14.73 kA	5.51 kA	723.09 kV(-31.13%)	0.26 s	32.98 MJ	**Interrupts**
	$t_d = 1.5ms$	15.41 kA	5.56 kA	719.83 kV(-31.44%)	0.27 s	36.07 MJ	**Interrupts**
	$t_d = 2ms$	15.99 kA	5.56 kA	716 kV(-31.81%)	0.27 s	38.39 MJ	**Interrupts**
	$t_d = 2.5ms$	16.62 kA	5.51 kA	715.35 kV(-31.87%)	0.26 s	40.63 MJ	**Interrupts**
	$t_d = 3ms$	17.48 kA	5.56 kA	719.83 kV(-31.44%)	0.25 s	43.04 MJ	**Interrupts**
MPC with i_z^{Σ} control	$t_d = 1ms$	14.51 kA	5.06 kA	701.06 kV(-33.23%)	0.16 s	27.69 MJ	**Interrupts**
	$t_d = 1.5ms$	15 kA	5.06 kA	700.16 kV(-33.32%)	0.17 s	29.15 MJ	**Interrupts**
	$t_d = 2ms$	15.59 kA	5.07 kA	701.49 kV(-33.19%)	0.17 s	30.84 MJ	**Interrupts**
	$t_d = 2.5ms$	16.01 kA	5.05 kA	700.58 kV(-33.28%)	0.17 s	31.85 MJ	**Interrupts**
	$t_d = 3ms$	16.6 kA	5.05 kA	700.8 kV(-33.26%)	0.18 s	33.18 MJ	**Interrupts**

TABLE V
PERFORMANCE DIFFERENT CASES UNDER THE POLE-TO-POLE FAULT AT MMC2 TERMINAL.

pole-to-pole fault		Peak in $i_{dc,CB2P}$	Peak in $i_{dc,MMC2}$	Undershoot in V_{dc}	settling time of V_{dc}	Pk Energy SA	Status
PI without i_z^{Σ} control	$t_d = 1ms$	39.26 kA	14.71 kA	-20.01 kV (101.91%)	Inf	0 MJ	**Fails**
	$t_d = 1.5ms$	39.14 kA	14.66 kA	-19.1 kV (-101.82%)	Inf	0 MJ	**Fails**
	$t_d = 2ms$	39.09 kA	14.61 kA	-20.47 kV (-101.95%)	Inf	0 MJ	**Fails**
	$t_d = 2.5ms$	39.09 kA	14.64 kA	-20.16 kV (-101.92%)	Inf	0 MJ	**Fails**
	$t_d = 3ms$	39.19 kA	14.67 kA	-19.53 kV (-101.86%)	Inf	0 MJ	**Fails**
MPC without i_z^{Σ} control	$t_d = 1ms$	35.42 kA	16.22 kA	-44.7 kV (-104.26%)	Inf	0 MJ	**Fails**
	$t_d = 1.5ms$	35.31 kA	16.08 kA	-40.77 kV (-103.88%)	Inf	0 MJ	**Fails**
	$t_d = 2ms$	35.15 kA	15.85 kA	-33.77 kV (-103.22%)	Inf	0 MJ	**Fails**
	$t_d = 2.5ms$	35.11 kA	15.46 kA	-29.99 kV (-102.86%)	Inf	0 MJ	**Fails**
	$t_d = 3ms$	34.94 kA	15.25 kA	-19.57 kV (-101.86%)	Inf	0 MJ	**Fails**
PI with i_z^{Σ} control	$t_d = 1ms$	15.25 kA	4.98 kA	324 kV (-69.14%)	0.27 s	39.34 MJ	**Interrupts**
	$t_d = 1.5ms$	16 kA	5 kA	324.31 kV (-69.11%)	0.27 s	42.87 MJ	**Interrupts**
	$t_d = 2ms$	16.75 kA	4.98 kA	323.68 kV (-69.17%)	0.25 s	46.39 MJ	**Interrupts**
	$t_d = 2.5ms$	17.56 kA	5.01 kA	324.28 kV (-69.12%)	0.24 s	49.49 MJ	**Interrupts**
	$t_d = 3ms$	18.63 kA	4.98 kA	324.24 kV (-69.12%)	0.22 s	53.77 MJ	**Interrupts**
MPC with i_z^{Σ} control	$t_d = 1ms$	15.15 kA	4.97 kA	307.95 kV (-70.67%)	0.23 s	32.88 MJ	**Interrupts**
	$t_d = 1.5ms$	15.89 kA	5.04 kA	307.74 kV (-70.69%)	0.18 s	35.64 MJ	**Interrupts**
	$t_d = 2ms$	16.57 kA	5.04 kA	307.95 kV (-70.67%)	0.18 s	38.52 MJ	**Interrupts**
	$t_d = 2.5ms$	17.26 kA	5.04 kA	307.61 kV (-70.7%)	0.18 s	40.45 MJ	**Interrupts**
	$t_d = 3ms$	17.99 kA	5.11 kA	308.5 kV (-70.62%)	0.18 s	42.86 MJ	**Interrupts**

the dc grid. The proposed control ensures the same energy absorption in the surge arrester during terminal PP and PG faults at converter, which regulates the dc voltage of MTdc. The proposed controller can also be added to the existing control strategies. However, the slower nature of the existing control strategies causes a larger setting time of the dc voltage.

There is a trade-off between the dc link voltage and the fault current. Based on the priority, suitable constraints in the controls need to be set up. However, the implementation of this control reduces the time dependence on the protection algorithm, breaker operation, and fault current limiters by increasing the reaction time window. Hence, it provides more time for the proper reaction of the dc CB during the dc fault. Furthermore, the energy absorption during the fault is reduced. Therefore, the footprint of the dc CB is reduced, and, thus, provides a low-cost solution.

More work will be done in the near future to investigate the sensitivity of this control on the latency, converter parameters and topology change. Besides, the constraints depending upon the system and fault conditions will be defined by taking into account the dc CB protection.

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