An Accelerated Detailed Equivalent Model for Modular Multilevel Converters

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Abstract—Detailed Equivalent Models (DEMs) of Modular Multilevel Converters (MMCs) are generally developed based on Thevenin equivalent circuits with a time-varying resistor. This approach may become computationally inefficient, specifically for the simulation of large power systems with many nodes, where the network admittance matrix needs to be frequently re-inverted every time a switching event occurs. This paper proposes a novel strategy to eliminate admittance matrix re-inversions during the converter's normal operation and restrict it only to when the converter undergoes blocking. The proposed DEM thus yields marked reductions in the simulation time of MMC circuits, and is particularly useful in studies wherein repetitive simulations are necessary. Models are implemented for MMCs with half-bridge (HBSM) and full-bridge (FBSM) sub-modules in the PSCAD/EMTDC simulator, and their accuracy is thoroughly validated for normal and blocked operating conditions. It is shown that the developed models are 30% and 60% more computationally efficient, respectively, for HBSM and FBSM MMCs in comparison to existing DEMs.

Keywords—Modular multilevel converters, detailed equivalent models, electromagnetic transient simulation.

I. INTRODUCTION

MODULAR multilevel converters are widely used in HVDC transmission systems. In comparison to two- or three-level converters [1], they have important advantages such as modularity, scalability, low harmonics, and reduced switching losses [2], [3]. MMCs generate output voltage waveforms with low harmonics by stacking building blocks, known as sub-modules (SMs), which make it possible to closely follow the reference waveform. Half-Bridge and Full-Bridge sub-modules (HBSMs and FBSMs) are by far the most commonly used sub-module types for they consist of a relatively small number of switches and have an inherent ability to block DC fault currents, respectively.

Computer simulation models of MMCs play critical rules in power system studies. The model needs to both accurately and efficiently represent the dynamics of the converter under normal and faulted operating conditions. However, the large number of switches in MMCs imposes a significant computational burden for EMT-type simulators if the MMC were to be modeled with connection of individual switches, known as a Detailed Switching Model (DSM). In such a

case, a prohibitively large network admittance matrix must be inverted every time a switching event occurs. Thus DSMs are usually used for very specific applications or MMCs with a low number of SMs, e.g., as in [4]. To overcome this, several equivalent models have been introduced that represent the dynamic response of the MMC while alleviating its computational burden. The Averaged-Value Model (AVM) proposed in [5], [6] is a popular model, which is suitable for low-frequency analysis of MMCs in normal mode of operation. This model has been used for system-level and controller design studies, e.g., for suppression of circulating currents [7], [8]. It is also useful for the analysis of the voltage ripple in capacitors and sizing them [9]. Although AVMs are generally intended to study the terminal behavior of the MMCs, several works [10]–[14] have introduced improved AVMs that include the blocking mode as well (see Table I). The main drawback of AVMs is that a single equivalent capacitor is used to characterize the stack of SMs in the arm, which prevents the study of individual capacitor voltages.

Detailed Equivalent Models (DEMs), on the contrary, efficiently represent MMCs in full detail and with an accuracy equal to a DSM. The core idea in a DEM is to replace the stack of SMs with a Thevenin or Norton equivalent circuit, which reduces its hundreds of nodes to two or three, thus diminishing the size of the network admittance matrix by many orders of magnitude. The Thevenin or Norton resistor and source parameters are affected by the numerical integration method employed for discretizing the voltage and current of the SM capacitors. Using trapezoidal integration method, references [15]–[20] and [21], [22] have developed DEMs with Thevenin and Norton equivalent circuits. Although these models offer remarkable computational efficiency compared with a DSM, the network admittance matrix must still be modified frequently, which makes re-triangularization of the admittance matrix, albeit a smaller one, unavoidable at every switching instant. In a large power network, this is highly problematic as the admittance matrix of the entire network needs to be inverted frequently only because of the presence of even one MMC. This is further aggravated in networks wherein several MMCs are present, e.g., in modern renewable-intensive systems.Even if a network with long transmission lines is split into different areas to reap the benefit of braking the conductance matrix of the large network into independent sub-matrices, each sub-matrix still needs to be re-factorized frequently if the MMC model is constructed with the time-varying resistance.

To overcome this major drawback, this paper proposes an approach to achieve a constant network admittance matrix that is re-inverted only when the converter blocking mode

TABLE I
SUMMARY OF MMC MODELS IN THE LITERATURE

Ref.	Model type			SM type(s)	Ability for blocked mode simulation	Focus of study
	DSM	DEM	AVM			
[4]	✓			HBSM	✓	Dynamic performance of MMC with 6 SM per arm
[5]			✓	N/A		Simplified HVDC model for analysis of MMC's dynamic behavior
[6]			✓	HBSM		Dynamics of MMCs based on terminal behavioral model
[10]			✓	HBSM	✓	Improved AVM model for simulation of DC fault condition
[11]			✓	HB,FB,MB-SM	✓	AVM model for the MMC operating at both blocked and normal mode
[12]			✓	HB,FB,CD-SM	✓	AVM model for the MMC operating at both blocked and normal mode
[13]			✓	HBSM	✓	401-Level MMC–HVDC System
[14]	✓	✓	✓	HBSM	✓	Comparison of MMC Models
[15]	✓	✓		HBSM	✓	First introduction to DEM. 24 SMs for validation of DEM against DSM
[16]		✓		HBSM	✓	Multi-terminal DC system
[17]		✓		HBSM	✓	Enhanced equivalent model
[21]	✓	✓		Two-port	✓	Multi-port SM structures. 8 SMs per arm for validation of DEM against DSM
[22]		✓		HBSM	✓	Current source MMCs. The dual circuit of conventional HBSM is used
[18]		✓		HBSM-BESS	✓	MMCs with embedded energy storage systems
[19]		✓	✓	HB,FB,CD-SM	✓	Combination of DEM and AVM models for fast and accurate simulation
[20]		✓	✓	HBSM-BESS	✓	MMCs with embedded energy storage systems

is invoked, e.g., in a DC fault. Since converter blocking is a rare event, the resulting converter model yields significant computational gains over existing DEMs, while retaining the ability to represent the converter during both normal and blocked conditions. The important contribution of this paper is the development of accelerated DEMs for MMCs with both HB and FB sub-modules that significantly reduce the EMT simulation time of networks with several MMCs. Furthermore, the proposed approach can be readily adopted for modeling emerging topologies of sub-modules as well.

The paper proceeds with continuous-time modeling of MMCs in Section II, and their discretization in Section III. An algorithm is then introduced by which the model can be implemented in an EMT solver. Model validation and results of simulation studies are presented in Section IV, followed by the conclusion in Section V.

II. MODELING OF THE CONVERTER'S ARM

As shown in Fig. 1, the arm in an MMC is a series connection of SMs carrying the arm current $i_{\mathrm{arm}}(t)$. The arm voltage $v_{\mathrm{arm}}(t)$ is equal to the summation of the SM voltages:

$$v_{\mathrm{arm}}(t) = \sum_{k=1}^{N} v_k(t) \tag{1}$$

where $v_k(t)$ is the voltage of the kth SM. The voltage produced by each SM is dependant upon the SM's topology, switching state, and capacitor voltage. In this paper, the most common types of SMs, i.e., HBSM and FBSM, shown in Fig. 1 (b) and (c), are considered.

A. Analysis of the MMC with HBSM

In normal mode of operation SMs are inserted or bypassed according to a modulation waveform, and the upper and lower switches of each SM are operated in a complementary manner. If the switching function for the kth SM is defined as

$$S_k(t) = \begin{cases} 1 & T_{1k}: \text{on}, T_{2k}: \text{off} \\ 0 & T_{1k}: \text{off}, T_{2k}: \text{on} \end{cases} \tag{2}$$
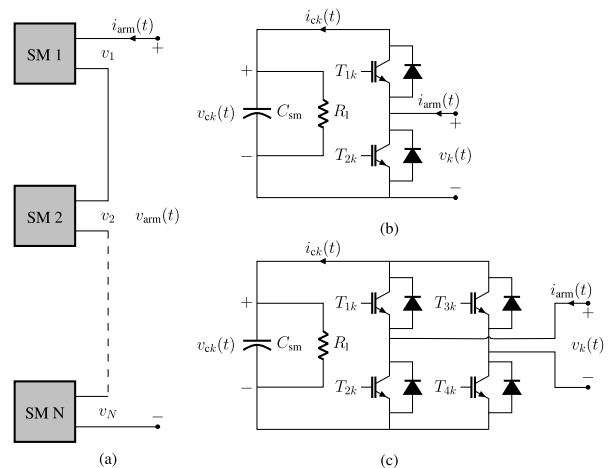

Fig. 1. (a): Stack of submodules in the arm, (b): Half-Bridge Sub-Module, and (c): Full-Bridge Sub-Module

then the current of the kth capacitor, $i_{\mathrm{c}k}(t)$, can be written as

$$i_{\mathrm{c}k}(t) = S_k(t)i(t) \tag{3}$$

where $i(t)$ is the current of the inserted SMs, which is equal to the arm current $i_{\mathrm{arm}}(t)$ in the normal mode. Note that the $i(t)$ and $i_{\mathrm{arm}}(t)$ represent different currents in the blocked mode even though they are the same in the normal mode of operation. The total voltage created by the inserted HBSMs in the arms has a component, $v_{\mathrm{tot}}^{\mathrm{n}}(t)$, which is contributed by the SM capacitors and depends on the SM's switching function, and may be expressed as follows:

$$v_{\mathrm{tot}}^{\mathrm{n}}(t) = \sum_{k=1}^{N} S_k(t)v_{\mathrm{c}k}(t) \tag{4}$$

where superscript 'n' denotes the normal mode of operation and subscript 'tot' represents the total voltage created. Additionally, in the path of the arm current through each SM, there is one resistor, either from the top or the bottom
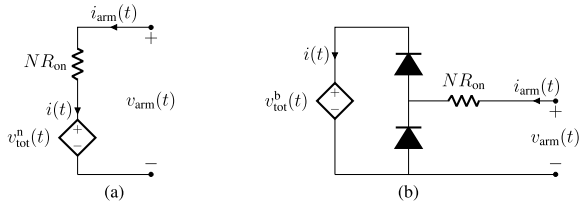
Fig. 2. Arm stack model with HBSM, (a): normal mode and (b): blocked mode.

switch-diode combination. Therefore, the total voltage across the arm is obtained by adding a resistive voltage drop to (4):

$$v_{\text{arm}}(t) = NR_{\text{on}}i(t) + v_{\text{tot}}^{\text{n}}(t) \qquad (5)$$

where R_{on} is an equivalent on-state resistance of a switch, and is considered to be the same for IGBTs and anti-parallel diodes, as is commonly done in EMT-type models.

In the blocked mode, all IGBTs are turned off and only the freewheeling diodes conduct the current. The arm stack may be viewed as a half-bridge diode rectifier with a series connection of all SM capacitors. The total voltage across the capacitors is the summation of the individual voltages of the capacitors, shown in Fig. 2, which share the same current $i(t)$. Therefore,

$$i_{\text{c}k}(t) = i(t) \qquad ; \qquad \forall k \qquad (6)$$

$$v_{\text{tot}}^{\text{b}}(t) = \sum_{k=1}^{N} v_{\text{c}k}(t) \qquad (7)$$

where superscript 'b' denotes the blocked mode. It must be noted that the equivalent diodes depicted in Fig. 2 are ideal.

The equivalent circuits in the normal and blocked modes can be amalgamated to a single circuit by adding an extra controlled switch that retains the same on-state resistance of NR_{on}. This is illustrated in Fig. 3 where the switch is controlled with the blocking signal. As long as the arm operates in normal mode, the switch is turned on and, with the anti-parallel diode, inserts the voltage source, $v_{\text{cap}}(t)$, into the path of the current. In the blocked mode of operation, the controlled switch is turned off and the circuit becomes a half-bridge diode rectifier. With this configuration, the following equations which describe the v-i characteristics of the dependent voltage source, accompanied with the circuit diagram in Fig. 3, which includes two diodes, one IGBT, and a resistor fully express the behavior of the arm stack with the HBSM topology:

$$i_{\text{c}k}(t) = \left(b(t) + \bar{b}(t)S_k(t) \right) i(t) \qquad (8)$$

$$v_{\text{tot}}(t) = \sum_{k=1}^{N} \left(b(t) + \bar{b}(t)S_k(t) \right) v_{\text{c}k}(t) \qquad (9)$$

$$i_{\text{c}k}(t) = C_{\text{sm}}\frac{\mathrm{d}v_{\text{c}k}}{\mathrm{d}t} + \frac{v_{\text{c}k}}{R_{\text{l}}} \qquad (10)$$

where C_{sm} is the SM capacitance, R_{l} is its leakage resistance and $b(t)$ is the blocking signal, which is equal to zero and one for normal and blocked modes, respectively. The signal $\bar{b}(t)$ is the complement of $b(t)$.
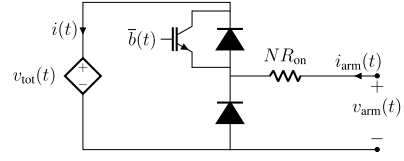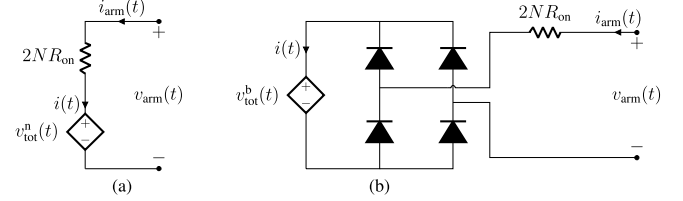

Fig. 3. Arm stack model with HBSM.

Fig. 4. Arm stack model with FBSM, (a): normal mode and (b): blocked mode.

B. Analysis of the MMC with FBSM

Two switching functions are required to model the behavior of each FBSM in the normal mode of operation. These switching functions are defined as follows, where T_{1k}-T_{4k} refer to the corresponding switches in Fig. 1(c).

$$S_{1k}(t) = \begin{cases} 1 & T_{1k}\text{: on}, T_{2k}\text{: off} \\ 0 & T_{1k}\text{: off}, T_{2k}\text{: on} \end{cases} \qquad (11)$$

$$S_{3k}(t) = \begin{cases} 1 & T_{3k}\text{: on}, T_{4k}\text{: off} \\ 0 & T_{3k}\text{: off}, T_{4k}\text{: on} \end{cases} \qquad (12)$$

The current of the kth capacitor may be expressed as:

$$i_{\text{c}k}(t) = (S_{1k}(t) - S_{3k}(t))i_{\text{arm}}(t) \qquad (13)$$

and the total voltage produced by the arm stack is

$$v_{\text{tot}}^{\text{n}}(t) = \sum_{k=1}^{N} (S_{1k}(t) - S_{3k}(t))v_{\text{c}k}(t) \qquad (14)$$

Taking the on-state resistance of each switch into account, the equivalent circuit of the arm stack is derived as depicted in Fig. 4(a). In the blocked state, all IGBTs are turned off and the arm stack is reduced to a full-bridge diode rectifier whose capacitor is the series connection of the individual sub-module capacitors, as shown in Fig. 4(b), where the capacitor is equivalently shown with a dependent voltage source $v_{\text{tot}}^{\text{b}}(t)$. The total voltage across the capacitors is the summation of the individual voltage of the capacitors, which share the same current $i(t)$. Therefore,

$$i_{\text{c}k}(t) = i(t) \qquad ; \qquad \forall k \qquad (15)$$

$$v_{\text{tot}}^{\text{b}}(t) = \sum_{k=1}^{N} v_{\text{c}k}(t) \qquad (16)$$

The equivalent circuits in Figs. 4(a)-(b) can be combined into a single circuit by connecting them together in series as illustrated in Fig. 5. It should be noted that the corresponding voltage source in each state, i.e., normal or blocked, will be active and the other will be bypassed. Therefore, the following
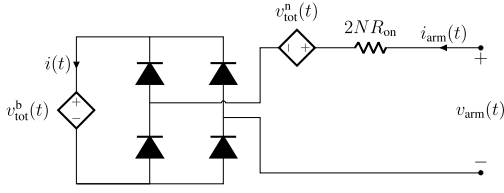
Fig. 5. Arm stack model with FBSM.

equations accompanied with the circuit in Fig. 5 fully describe the behavior of the arm stack of an MMC with FBSM.

$$i_{ck}(t) = b(t)(S_{1k}(t) - S_{3k}(t))i_{\text{arm}}(t) + \overline{b}(t)i(t) \qquad (17)$$

$$v_{\text{tot}}^{\text{n}}(t) = b(t)\sum_{k=1}^{N}(S_{1k}(t) - S_{3k}(t))v_{ck}(t) \qquad (18)$$

$$v_{\text{tot}}^{\text{b}}(t) = \overline{b}(t)\sum_{k=1}^{N}v_{ck}(t) \qquad (19)$$

$$i_{ck}(t) = C_{\text{sm}}\frac{dv_{ck}}{dt} + \frac{v_{ck}}{R_{\text{l}}} \qquad (20)$$

Note that all equations derived in this section represent the respective models of the HBSM and FBSM stack topologies and, by nature, all voltages and currents are not known until all equations are discretized and interfaced with the EMT solver.

III. DISCRETIZATION OF THE GOVERNING EQUATIONS

In this section the governing equations of the arm stack derived in section II are discretized. Euler's method of integration is used, as it models the capacitor with only an equivalent history voltage source that is dependent on the voltage and current at the previous time-step. Thus, there exists no resistor in the Thevenin equivalent circuit of the capacitor. In turn, the whole arm model, which inserts or bypasses the SM capacitors based on the switching functions, does not manifest a time-varying resistor in its Thevenin equivalent circuit. As a result, there is no change in the elements of the network admittance matrix and, hence, no requirements for its re-inversion. Note that part of the computational advantage of this method arises from the fact that instead of finding a Thevenin equivalent for every SM and putting them in series, as is done in conventional DEMs, the SM capacitor voltage's equations (see (20)) is directly integrated numerically and shown as a voltage source. The voltages from all SM capacitors are then added together, to which the resistive voltage drop of the semiconductors is also added (see (5)). In existing DEMs, which are developed based on the trapezoidal rule of integration, however, the Thevenin resistance of the inserted SM capacitors are summed up to achieve the whole arm model, thereby yielding a time-depedent resistor, which varies with the switching functions of the SMs. Accordingly, the network admittance matrix needs to be re-triangularized every time the switching functions change.

Using (10) or (20), the capacitor's voltage at the present time-step can be calculated from the previous time-step values as:

$$v_{ck}(t) = k_{\text{e}}v_{ck}(t - \Delta t) + R_{\text{e}}i_{ck}(t - \Delta t) \qquad (21)$$

where Δt is the simulation time-step, and the parameters k_{e} and R_{e} are defined as follows:

$$k_{\text{e}} = 1 - \frac{\Delta t}{R_{\text{l}}C} \qquad \text{and} \qquad R_{\text{e}} = \frac{\Delta t}{C} \qquad (22)$$

The capacitor voltages $v_{ck}(t - \Delta t)$ are known values from the past solution of the network. However, the capacitor currents $i_{ck}(t - \Delta t)$ are not explicitly known and must be calculated using (8) and (17) by substituting $t - \Delta t$ for t. Thus the capacitor currents at the previous time-step are calculated for HBSM and FBSM as in (23) and (24), respectively.

$$i_{ck}(t - \Delta t) = \big(b(t - \Delta t) + \overline{b}(t - \Delta t)S_k(t - \Delta t)\big) \\ \times i(t - \Delta t) \qquad (23)$$

$$i_{ck}(t - \Delta t) = b(t - \Delta t)(S_{1k}(t - \Delta t) - S_{3k}(t - \Delta t)) \\ \times i_{\text{arm}}(t - \Delta t) + \overline{b}(t - \Delta t)i(t - \Delta t) \qquad (24)$$

Finally, the total voltage can be calculated by substitution of (21) in (14) and (18)-(19) for HBSM and FBSM sub-modules, respectively. For instance, the total voltage for HBSM topology is expressed as

$$v_{\text{tot}}(t) = \sum_{k=1}^{N} \Bigg[\bigg(b(t) + \overline{b}(t)S_k(t)\bigg) \times \bigg(k_{\text{e}}v_{ck}(t - \Delta t) + \\ R_{\text{e}}\big(b(t - \Delta t) + \overline{b}(t - \Delta t)S_k(t - \Delta t)\big) \times i(t - \Delta t)\bigg) \Bigg]$$
$$(25)$$

The HB and FB DEMs developed so far could be connected in series or other types of connections to build an arm model of a hybrid MMC configuration as long as the fundamental building blocks, i.e. sub-modules, of the new topology are either HBSM or FBSM. For other SM types, the same approach may be taken to the develop the DEM.

With the discretized equations, Fig. 6 shows the flowchart of an algorithm by which the arm stack is built in an EMT-type simulation platform.

IV. SIMULATION RESULTS

The arm equivalent circuits derived in section II are implemented in the PSCAD/EMTDC simulator [23], [24] for both HBSM and FBSM sub-modules. Several case studies are carried out to evaluate the performance of the proposed models, particularly to (i) establish their accuracy, and (ii) assess their computational advantage over existing DEMs. A simple test system comprising a single MMC connected to an infinite bus via a reactance is considered first. This example serves to validate the steady state operation of the converter and its response to a pole-to-pole (PTP) dc fault. Simulation results from this case are compared against those from the existing DEM in PSCAD/EMTDC to verify the accuracy of the proposed models. Next three CIGRE B4-57 MMC-HVDC grids [25], [26] are considered, in which several MMCs are embedded in increasingly more complex dc grids.

It must be noted that existing commercially available DEMs have been heavily used over the past decade by manufacturers, utilities, and consulting engineers, and are known to be
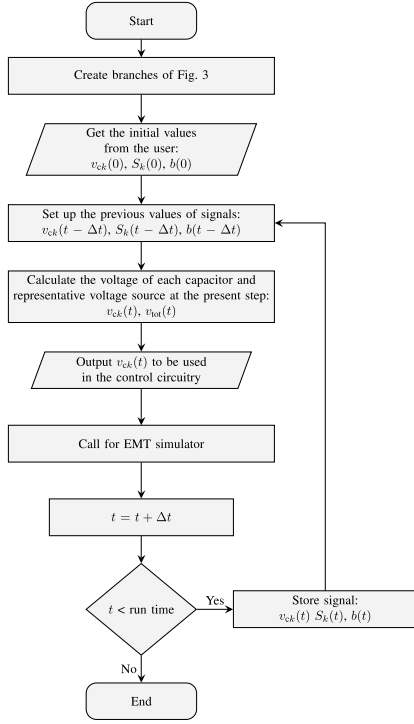
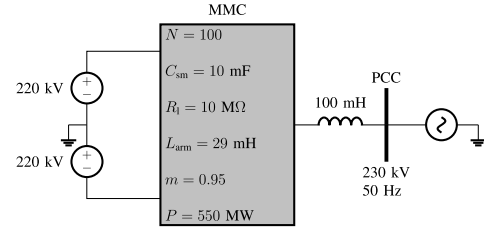Fig. 6. Flowchart of simulations using the proposed HBSM model.
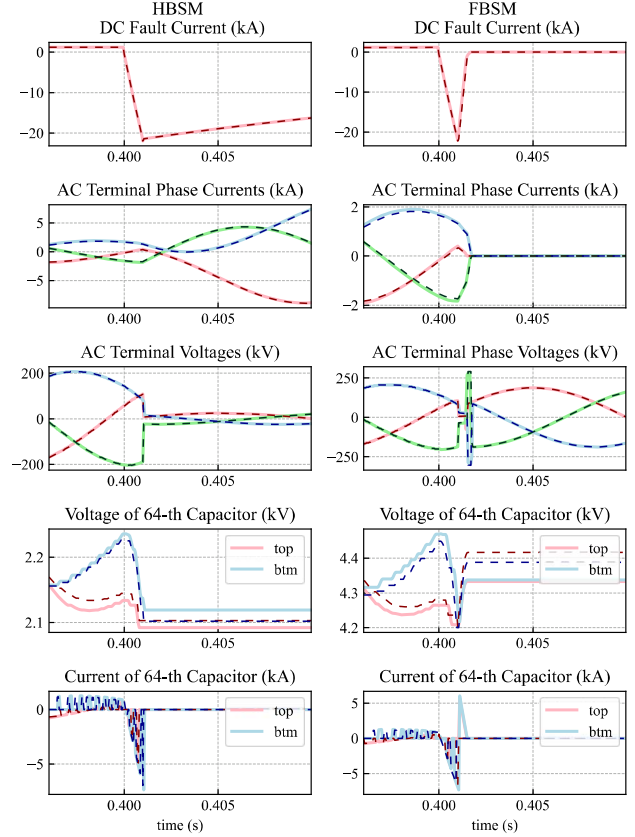

Fig. 7. Circuit diagram of the system in case study 1.

Fig. 8. Case study 1: Waveform for a PTP fault for HBSM and FBSM topologies. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.

accurate in representing the behavior of an actual MMC. They have also been verified against analytical and experimental results [27]. This is why they are used as the benchmark to validate the models proposed in this paper.

A. Case Study 1: Single-MMC Circuit

The circuit diagram of the simple test system used for accuracy verification of the proposed models is shown in Fig. 7. The MMC is operated with the DC side voltage of 440 kV and 95% modulation index, producing a line-to-line voltage of 256 kV at its AC terminal. The produced voltage leads the PCC voltage by 17.2° to deliver 550 MW of real power to the power system. A PTP fault is applied at $t = 0.4$ s and the converter is blocked 1 ms thereafter. The circuit is simulated with both HBSM and FBSM topologies, with a simulation time-step of 50 μs. Fig. 8 shows the waveform of the dc fault current, ac terminal voltage and current, and voltage and current of a randomly selected SM capacitor (64th) from the top and bottom arm for both HBSM and FBSM circuits. After the fault is cleared, the system settles at a new operating condition for which the arm currents, summation of capacitors voltages in each arm, and voltage and current of a random SM (31th) are shown in Fig. 9. Except for slight discrepancies in the SM-level waveforms, the results produced by the proposed models (dashed lines) match those by the existing DEM (solid lines), thus they verify the accuracy of the proposed models during both steady state and faulted conditions. Slight differences in the SM-level quantities are due to the small differences in the sorted SM capacitor lists submitted to the firing pulse controller.

B. Case Study 2: CIGRE MMC-HVDC Benchmarks

Three simulation models of the CIGRE B4-57 MMC-HVDC grids [25], [26] with 2, 4, and 16 MMCs are considered. Specifications of the systems and their parameter values may be found in [26]; they are not repeated here for brevity. In all simulations in this section, the MMCs are considered to have the same number of sub-modules. Two tests, as elaborated upon below, are conducted to evaluate the performance of the proposed models.

1) Test I: The MMC-HVDC network with 4 MMC units is considered for this test. The single-line diagram of this network is shown in Fig. 10. Each arm of the MMCs in the network consists of 200 HBSM sub-modules with a 10000 μF SM capacitor. The network is simulated twice, once with the existing DEM in PSCAD/EMTDC as the benchmark and
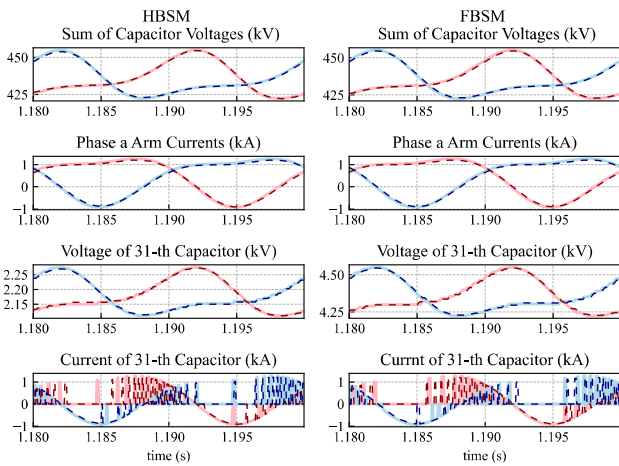
Fig. 9. Case study 1: Waveforms of MMC during normal mode. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.
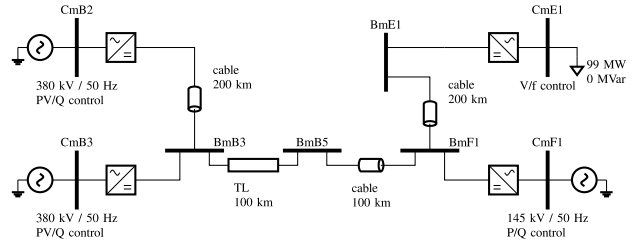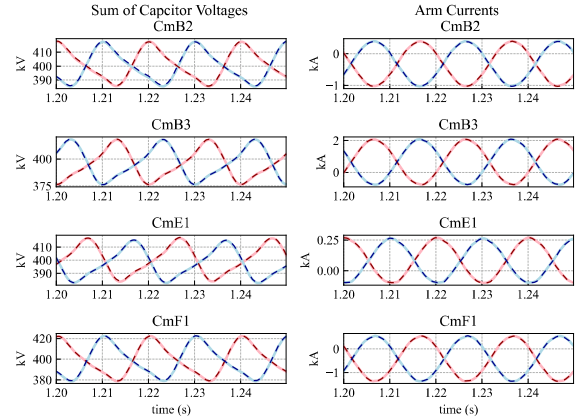

Fig. 10. CIGRE B4-57 MMC-HVDC grid with 4 MMC stations.

Fig. 11. Case study 2 (Test I): Arm currents and summation of capacitor voltages. solid: PSCAD/EMTDC's existing DEM, line: proposed model.

once with the proposed DEM. Fig. 11 shows the arm currents and summation of the capacitor voltages for phase-a of each converter station in steady state. A negative step change of 200 MW is applied at $t = 1.5$ s to the converter at bus CmF1, followed by a positive 300 MW step change at $t = 2.0$ s. The variations of the measured power at the dc terminals of the converter stations are shown in Fig. 12. A permanent PTP fault is applied at the converter station CmF1 at $t = 2.5$ s. The voltage and current waveforms of the dc terminals of each converter station are shown in Fig. 13. As clearly seen, the waveforms from the existing PSCAD/EMTDC's DEM match perfectly with those produced by the proposed model, thus further validating its accuracy.

2) Test II: Each of the MMC-HVDC grid models, i.e. with 2, 4, and 16 MCCs, is simulated with different number of SMs using both the proposed and PSCAD/EMTDC's existing DEM. In order to achieve the same dynamic responses as the number of SMs is varied, the SM capacitance is updated so that the equivalent arm capacitance, $C_{arm} = C_{sm}/N$, remains constant at $50\,\mu$F. The simulation time-step and run duration are $50\,\mu$s and 2 s, respectively. Simulations are conducted on a computer with 3.40 GHz Intel Core i7-6700 CPU with 16 GB of memory. To eliminate the effect of run-time plotting of waveforms on the recorded CPU time, all figures (graphs) are removed after first having confirmed that the resulting waveforms are accurate. Table II shows the measured CPU run-time in seconds for systems with different number of MMCs and sub-modules for HBSM topology. The tests are also repeated for the same systems with FBSMs with proper control circuitry, and the results are tabulated in Table III. To compare the effectiveness of the proposed model, the ratio of its CPU run-times to those of the PSCAD/EMTDC's DEM is plotted against the number of sub-modules in Fig. 14.
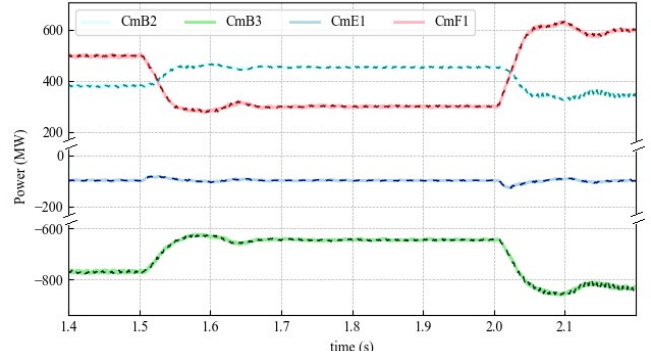

Fig. 12. Case study 2 (Test I): Measured power in converter stations. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.
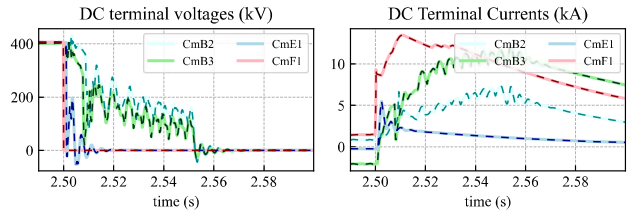

Fig. 13. Case study 2 (Test I): Measured DC voltages and currents in converter stations. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.

The graph shows the run-time ratio for different number of MMCs in the network for both HBSM and FBSM configurations. The graphs show significant reductions in CPU time by the proposed models. For 200 HBSMs per arm, for example, the proposed model is around 30% more

TABLE II
CPU Run-Time of MMC-HVDC Systems with HBSM

N_{MCC}	2		4		16	
N_{sm}	Proposed	Existing	Proposed	Existing	Proposed	Existing
50	3.7	8.8	7.3	16.5	38.9	96.4
100	6.4	12.9	12.7	23.5	52.6	116
150	10.6	17.8	21.7	33.1	81.3	152
200	16.2	24.1	31.9	44	117	185
250	23.7	32.4	45.7	58.9	165	239
300	32.5	41.9	62.3	76.6	210	289
350	43.1	52.3	85.8	99.4	298	375
400	50	65.2	104	117	383	431

TABLE III
CPU Run-Time of MMC-HVDC Systems with FBSM

N_{MCC}	2		4		16	
N_{sm}	Proposed	Existing	Proposed	Existing	Proposed	Existing
50	4.3	15.2	8.7	29.1	62.1	139
100	6.7	24.6	13.1	43.4	77.3	200
150	10.9	35.3	22.3	62.2	104	279
200	16.7	47.5	31	84.7	145	354
250	23.7	62.8	42.5	110	181	455
300	32.4	75.7	59.4	137	254	567
350	40.1	90.9	78.4	162	307	646
400	52.3	107.6	93	197	371	753

Fig. 14. Ratio of CPU run-time of the proposed models to the existing DEMs.

Fig. 15. Network modeled with mixed integration method

computationally efficient than the existing DEM. For 200 FBSMs, however, it is more than 60% accelerated.

The CPU run-time is chiefly affected by two factors. One is the time needed for re-triangularization of the admittance matrix. The other is the time consumed for calculations of control signals for IGBTs' firing signals. In each run, the dimensional order of the admittance matrices remain constant and nearly the same for both the proposed model and the PSCAD/EMTDC's DEM. However, the number of control signals is approximately proportional to the number of sub-modules in each run. Therefore, for larger numbers of SMs, the CPU run-time is predominately determined by the number of sub-modules. Because control signal calculations are held the same for the cases with the proposed and existing DEMs, the ratio is expected to increase and approach unity when the number of the SMs increases, as is also seen in Fig. 14. The proposed models, however, show significant savings even for SM counts as high as 400, for which the proposed FBSM models are more than twice as fast as the existing DEM.

V. Numerical Stability and Accuracy

Euler's method of integration is not A-stable and will become numerically unstable if the time-step exceeds certain limits. This limit is determined by the maximum value of the eigenvalues of the discretized state-space matrix of the circuit provided that all state variables are discretized with the Euler's method. In this paper, however, only the stack of SMs are discretized with Euler's method and the rest of the circuit including the arm inductors, transmission lines, transformers, etc, are modeled with the trapezoidal method as shown in Fig.15(a). This mixture of integration methods is also not A-stable but its margin of stability is greater than that of the case where all components are constructed with the Euler's method.
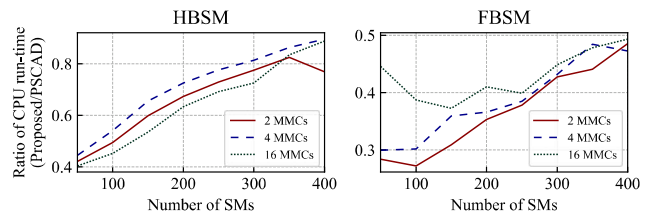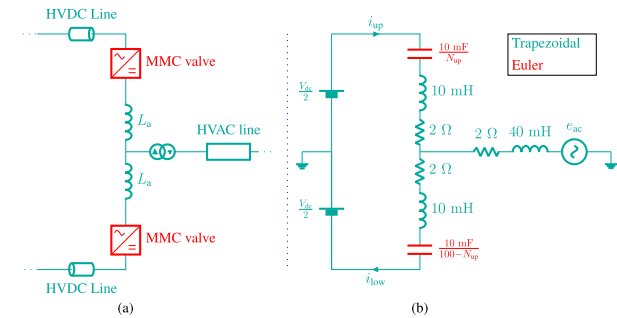
Fig.15(b) shows an example of an MMC with 100 SMs in normal mode in which, at every moment, N_{up} and $100 - N_{\text{up}}$ capacitors are inserted in the upper and lower arms, respectively. By performing circuit analysis, the state-space equation in the discrete domain may be written as follows:

$$\mathbf{X}(t) = \mathbf{G}(\Delta t)\mathbf{X}(t - \Delta t) + \text{effects of the inputs} \quad (26)$$

where $\mathbf{X}$ is the states and $\mathbf{G}$ is the discretized state-space matrix, which is a function of Δt. For all possible number of SMs inserted, the maximum time-step beyond which the simulations are numerically unstable are calculated and plotted in Fig.16. As shown, the worst-case maximum time-step is around 670 μs, which is 13 times larger than 50 μs, the typical time-step in power system applications.

For a network with switching elements the eigenvalues are not the only determinant of the maximum time-step. In fact, switching frequencies and time durations by which the circuit undergoes different states are of significant importance for if the time-step is not small enough, switching events will be missed. Heuristically, one tenth of the minimum switching period is considered for selecting the time-step.

In MMCs, the voltage generated by the stack of SMs is a staircase quantized sinusoidal waveform. Assuming that time intervals in the staircase waveform are equal, the length of each interval is $\frac{1}{Nf}$ where N and f are the number of SMs and frequency of the AC network, respectively. For instance, if the MMC has 100 SMs per arm and the AC network frequency is 60 Hz, the length of each interval would be $\frac{1}{100 \times 60} = 166.66$ μs meaning that the maximum time-step is 166.66 μs. Such a rough calculation is specifically useful for MMCs controlled by the Nearest Level Control method. In PWM-controlled MMCs the recommended time-step is one tenth of the switching period of the PWM signal. For
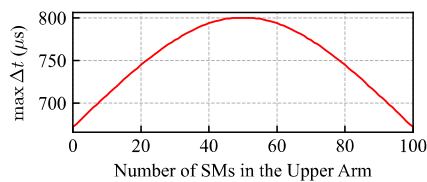
Fig. 16. Maximum time-step vs. number of SMs inserted from upper (lower) arm

example, if the PWM signal has a frequency of 1 kHz, the recommended time-step would be $\frac{1}{10 \times 1000} = 100$ μs. Hence, a typical time-step in MMC simulations does not usually exceed 150 μs and for a common time-step of 50 μs, it is highly unlikely that the proposed mixed integration method becomes numerically unstable or inaccurate for (i) all elements except the stack of SMs are modeled with the trapezoidal integration method and (ii) the time-step must be inherently small enough to avoid missing switching events. The results of simulation case studies presented in section IV validate the stability and accuracy of the proposed method.

VI. CONCLUSION

A DEM was introduced for EMT simulation of MMCs, based upon Thevenin equivalents of the arm stack. The new DEM features a constant conductance and alleviates modifications of the network admittance matrix except when the MMC enters or leaves the blocked mode of operation. The paper showed that using Euler's method does not adversely affect the accuracy or stability of the models, and that they are 30% and 60% more computationally efficient than existing DEMs for HBSM and FBSM, respectively. Several case studies were carried out whose results matched those from the existing DEM model in PSCAD/EMTDC.

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