Model Predictive Control for Solid State Transformer

A. F. Nardoto, A.E.A. Amorim, L. F. Encarnação, W.M. Santos, E.J. Bueno, D.M. Blanco

***Abstract*-- The solid-state transformer (SST) is being presented as a technology that enables the construction of new power systems due to its many advantages. These benefits include reduced weight and volume compared to traditional transformers, power factor compensation, accurate output voltage regulation, harmonic mitigation, short-circuit current limitation, and voltage dip immunity, under certain conditions. Unlike other studies that only demonstrated the effectiveness of Model Predictive Control (MPC) in individual parts of the SST, this study shows the control of an entire SST using the MPC strategy. The performance of the SST during power system transients is evaluated to showcase the features of the SST by predictive control.**

***Keywords*: DAB Converter, Finite Set – MPC, Inverter, Model Predictive Control – MPC, Multi-Level Converter, Rectifier, Solid State Transformer - SST.**

I. Introduction

THE emergence of renewable sources and new loads such as electric vehicles is changing the paradigm of the distribution grid. This new scenario, known as the smart grid, demands precise power control, incorporation of energy storage systems, easy integration of new sources, and quick response to transients. To meet these requirements, traditional transformers are becoming obsolete, and power electronics-based equipment is replacing them [1].

The solid-state transformer (SST) is a technology that enables the construction of new power systems. Some advantages of SST are reduced weight and volume compared to traditional transformers, power factor compensation, precise output voltage regulation, harmonic mitigation, short-circuit current limitation, and voltage dip immunity under certain limitations. However, SST has disadvantages related to its cost, reliability, and efficiency [2] [3].

All these benefits are found in the literature, and the benchmark topology for the SST is the modular multilevel topology based on input series and output parallel (ISOP) configuration, as it shares the voltage in series connection and current in parallel connection [4][5][6].

Moreover, many studies demonstrate the effective performance of Model Predictive Control (MPC) in each part of the SST: AC-DC [7][8], DC-DC [9], and DC-AC stages [10][11]. However, the control of an entire SST employing only the MPC strategy has not yet been demonstrated, presenting the interactions among all the SST stages. Furthermore, this study shows the decoupling between the control stages, showing that the MPC computational burden is not directly related to the SST size. The SST performance is evaluated during both steady and transient regimes. This study is organized as follows: Section II presents the SST mathematical model using the MPC approach, Section III demonstrates the proposed control strategy, Section IV shows the real-time simulation results, and Section V has the final considerations.

II. MPC - SST

In this section, the converter models employed in all the SSTs are presented. Fig. 1 shows the three-stage SST topology with *M* modules adopted in this study.

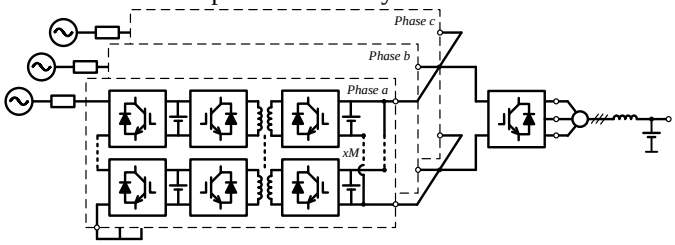

Fig. 1. Topology SST used in this work.

A. AC-DC stage model with delay compensation

Fig. 2 shows the AC-DC stage, or rectifier stage, used in this study. The rectifier consists of a full-bridge series configuration that enables the SST to connect directly to the medium-voltage grid (v_{MVAC}). By interlocking the switches on the same module leg, a total of $2^{(2.M)}$ different states can be achieved, where M represents the number of modules in the SST [12].

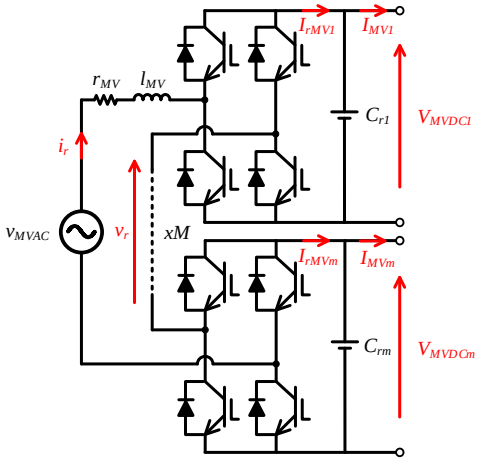

Fig. 2. Topology stage AC/DC used in SST: Full bridge series connected.

This study was supported by National Council for Scientific and Technological Development – CNPq (grant numbers 409024/2021-0 and 311848/2021-4) and Espírito Santo Research and Innovation Support Foundation – FAPES (grant numbers 514/2021, 668/2022 and 1024/2022).

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Equation (1) is derived by applying Kirchhoff's Law to the AC side of the rectifier. In this Equation, l_{MV} represents the inductance of the rectifier's L filter, and r_{MV} represents the electrical losses in the inductor.

$$v_{MVAC} = r_{MV} i_r + l_{MV} \frac{di_r}{dt} + v_r \quad (1)$$

On the DC side of the rectifier, the voltage balance in each capacitor is directly related to its current flow. Thus, when $V_{MVDC1} = \cdots = V_{MVDCm} = V_{MVDC}$, the dynamic Equation of V_{MVDCm} can be obtained using (2).

$$C_{rm} \frac{dV_{MVDCm}}{dt} = I_{rMVm} - I_{MVm} \quad (2)$$

Where $C_{r1} = \cdots = C_{rm} = C_r$ represent the capacitances of each cell, and I_{rMVm} and I_{MVm} denote the input and output currents of the capacitor for each cell.

The predictive model is obtained by applying Euler discretization to the expressions in (1) and (2), resulting in (3) and (4), respectively.

$$i_r(k+1) = i_r(k) + \frac{T_s}{l_{MV}} \left(v_r^k - r_{MV} i_r(k) - v_{MVAC}(k)\right) \quad (3)$$

$$V_{MVDCm}(k+1) = V_{MVDCm}(k) + \frac{T_s}{C_{rm}} \left(S_M^k . i_r(k) - I_{MVm}(k)\right) \quad (4)$$

Where v_r^k and S_M^k represent the output voltage and rectifier module switch states at present values; T_s is time step; k and $(k+1)$ represent the measured and predicted values of the variables at time k and $(k+1)$, respectively.

A voltage will be synthesized at time $(k+1)$ based on the switching state defined at time k. During the time interval between k and $(k+1)$, calculations will be performed to estimate the voltages for the next cycle, which will occur at time $(k+2)$. To predict the voltages at time $(k+2)$, the voltage at time $(k+1)$ is calculated, which is called delay compensation. This is when the new switch state will be decided. Thus, all possible voltages that can be synthesized at time $(k+2)$ are based on the calculated voltage at time $(k+1)$. Similarly, the current at time $(k+2)$ is calculated. The predictive model is described in (5) and (6).

$$i_r^N(k+2) = i_r(k+1) + \frac{T_s}{l_{MV}} \left(v_r^N - r_{MV} i_r(k) - v_{MVAC}(k)\right) \quad (5)$$

$$V_{MVDCm}^N(k+2) = V_{MVDCm}(k+1) + \frac{T_s}{C_{rm}} \left(S_M^N . i_r(k+1) - I_{MVm}(k)\right) \quad (6)$$

Where $i_r^N(k+2)$ are the N predicted input current, v_r^N are the N output voltage possibilities, $V_{MVDCm}^N(k+2)$ are the N output voltage possibilities, S_M^N represents the M^{th} rectifier module switches states.

B. DC-DC stage model with delay compensation

Fig. 3 shows the DC-DC stage topology used in the SST. This stage is composed of several power modules that are connected in parallel on the LVDC grid side and by isolated sources on the MVDC grid side. Each module is an isolated Dual Active Bridge (DAB) converter. The active power transmitted by each module P_m is calculated using (7) [13].

$$P_m = V_{LVDC} \cdot I_{0Dm} = \frac{4 \cdot n \cdot V_{LVDC} \cdot V_m \cdot \sin \delta_m}{\pi^3 \cdot f_{sw} \cdot L_{km}} \quad (7)$$

Where m represents the m^{th} DAB converter, V_m and I_{0Dm} are the average values of the input voltage and output current of the m^{th} DAB converter, V_{LVDC} is the LVDC voltage, L_{km} is the power transfer inductance, n is the transformer ratio, $f_{sw} = 1/T_s$ is the switching frequency, and δ_m is the phase-shift of the primary and secondary square-wave voltages of the m^{th} DAB converter.

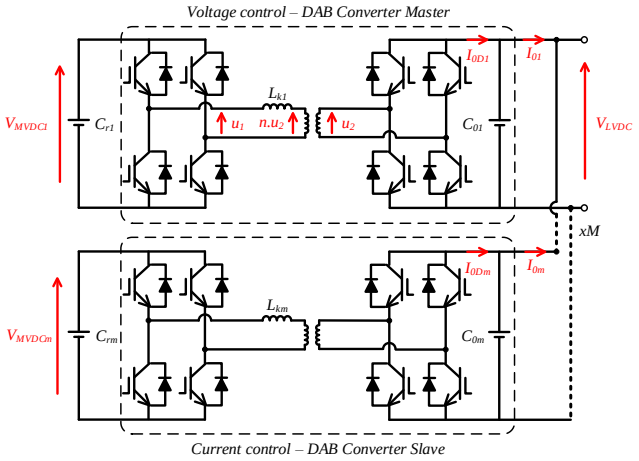

Fig. 3. DC-DC stage topology used in SST: DAB connected isolated sources on the MVDC grid side and in parallel on the LVDC grid side.

The direction of power flow is determined by the phase shift signal δ_m, where a positive value indicates power transfer from MVDC to LVDC, otherwise indicates the reverse flow [13].

The average value of capacitor output voltage is determined by the relationship between the currents of each capacitor, as described in (8).

$$C_{0m} \frac{d\langle V_{LVDC}\rangle_{T_s}}{dt} = \langle I_{0m}\rangle_{T_s} - \langle I_{0Dm}\rangle_{T_s} \quad (8)$$

Where I_{0Dm}, i_{0m}, and C_{0m} represent the input capacitor current, measured load current, and output capacitance of the m^{th} DAB converter, respectively.

The first converter, $m = 1$, is the master and controls the voltage on the LVDC bus. The output voltage prediction is defined by using the Euler method to discretize (8), resulting in (9).

$$V_{LVDC}(k+1) = V_{LVDC}(k) + \frac{I_{0D1}^k - I_{01}(k)}{C_{01} \cdot f_{sw}} \quad (9)$$

Where $i_{01}(k)$ and $V_{LVDC}(k)$ are measured at time k, and I_{0D1}^k is synthesized current at the output of the converter at time k, derived from (7).

Delay compensation is performed similarly to that used in rectifiers. The N possible output voltages at time $(k+2)$ are obtained from N output current possibilities I_{0D1}^N, as shown in (10).

$$V_{LVDC}^{N}(k+2) = V_{LVDC}(k+1) + \frac{I_{0D1}^{N} - i_{01}(k)}{C_{out} \cdot f_s} \tag{10}$$

The parallel connection of the DAB converters ensures that the voltages on the LVDC grid side are equal. Thus, to guarantee that all converters transmit the same power, it is necessary to ensure that their output currents are also equal, as shown in (11).

$$I_{01} = I_{02} = \cdots = I_{0m} \tag{11}$$

C. DC-AC stage model with delay compensation

Fig. 4 shows a Voltage Source Inverter (VSI) with a LC filter.

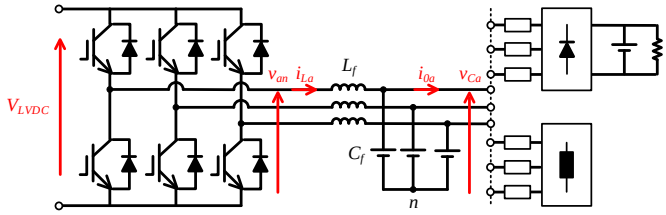

Fig. 4. Typical topology of an *LC*-filtered standalone VSI.

The VSI three-phase voltages can be represented by the αβ stationary frame by applying the Clarke transform. Thus, the capacitor voltage $\mathbf{V_{C\alpha\beta}}$, inductor current $\mathbf{I_{L\alpha\beta}}$, inverter voltage $\mathbf{V_{\alpha\beta}}$, and load current $\mathbf{I_{0\alpha\beta}}$ are:

$$\begin{aligned}
\mathbf{V_{C\alpha\beta}} &= v_{C\alpha} + j.v_{C\beta} = T_{3/2} \cdot [v_{Can} + v_{Cbn} + v_{Ccn}]^T \\
\mathbf{I_{L\alpha\beta}} &= i_{L\alpha} + j.i_{L\beta} = T_{3/2} \cdot [i_{La} + i_{Lb} + i_{Lc}]^T \\
\mathbf{V_{\alpha\beta}} &= v_{\alpha} + j.v_{\beta} = T_{3/2} \cdot [v_{an} + v_{bn} + v_{cn}]^T \\
\mathbf{I_{0\alpha\beta}} &= i_{0\alpha} + j.i_{0\beta} = T_{3/2} \cdot [i_{0a} + i_{0b} + i_{0c}]^T
\end{aligned} \tag{12}$$

Where,

$$T_{3/2} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{13}$$

The dynamic model of a second-order LC filter in continuous-time is presented in (14).

$$\begin{aligned}
\frac{d\mathbf{V_{C\alpha\beta}}}{dt} &= \frac{1}{C_f} \cdot (\mathbf{I_{L\alpha\beta}} - \mathbf{I_{0\alpha\beta}}) \\
\frac{d\,\mathbf{I_{L\alpha\beta}}}{dt} &= \frac{1}{L_f} \cdot (\mathbf{V_{\alpha\beta}} - \mathbf{V_{C\alpha\beta}})
\end{aligned} \tag{14}$$

Where L_f and C_f are filter inductance and capacitance.

The dynamics in Equation (14) indicates that the system state variables $\mathbf{I_{L\alpha\beta}}$ and $\mathbf{V_{C\alpha\beta}}$ exhibit a cross-coupling effect. The LC filter discrete predictive model that considers the cross-coupling is presented in [14] and expressed in (15).

$$\begin{bmatrix} \boldsymbol{I}_{L\alpha\beta}(k+1) \\ \boldsymbol{V}_{C\alpha\beta}(k+1) \end{bmatrix} = \begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{I_{L\alpha\beta}}(k) \\ \mathbf{V_{C\alpha\beta}}(k) \end{bmatrix} + \begin{bmatrix} \Gamma_{11} & \Gamma_{12} \\ \Gamma_{21} & \Gamma_{22} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{V_{\alpha\beta}}(k) \\ \mathbf{I_{0\alpha\beta}}(k) \end{bmatrix} \tag{15}$$

Where the coefficient matrices are calculated by

$$\begin{aligned}
&\Phi = e^{\boldsymbol{A} \cdot T_s}, \Gamma = \int_0^{T_s} e^{\boldsymbol{A} \cdot \tau} \cdot \boldsymbol{B} \cdot d\tau \\
&\boldsymbol{A} = \begin{bmatrix} 0 & -1/L_f \\ 1/C_f & 0 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} 1/L_f & 0 \\ 0 & -1/C_f \end{bmatrix},
\end{aligned} \tag{16}$$

Where T_s is the sampling time, $\boldsymbol{I}_{\mathbf{L\alpha\beta}}(k+1)$ and $\boldsymbol{V}_{\mathbf{C\alpha\beta}}(k+1)$ describe the current and voltage delay compensation at present values. $\boldsymbol{V}_{C\alpha\beta}(k)$ represents the measured capacitor voltage, $\boldsymbol{I}_{L\alpha\beta}(k)$ the measured inductor current, $\boldsymbol{I}_{0\alpha\beta}(k)$ the measured output current, and $\boldsymbol{V}_{\alpha\beta}$ the synthesized voltage at present values.

Delay compensation is similar to that used in rectifiers. The predicted capacitor voltage $\boldsymbol{V}_{C\alpha\beta}^{N}(k+2)$ is based on the $(k+1)^{th}$ predicted values in (15), as shown in (17).

$$\begin{aligned}
\mathbf{V_{C\alpha\beta}^{N}}(k+2) &= \Phi_{21} \cdot \boldsymbol{I}_{\mathbf{L\alpha\beta}}(k+1) + \Phi_{22} \cdot \boldsymbol{V}_{\mathbf{C\alpha\beta}}(k+1) \\
&+\Gamma_{21} \cdot \mathbf{V_{\alpha\beta}^{N}} + \Gamma_{22} \cdot \mathbf{I_{0\alpha\beta}}(k+1)
\end{aligned} \tag{17}$$

Where $\mathbf{V_{\alpha\beta}^{N}}$ represents the N output voltage possibilities from switches states. If dynamics of load current are slow, then $\mathbf{I_{0\alpha\beta}}(k+1) = \mathbf{I_{0\alpha\beta}}(k)$.

III. Proposed MPC Control

The serial and parallel connection of full bridges has been a strategy found in the literature to allow converters to operate at high voltages and powers. When multiple converters operate concurrently in an MPC application, many switching states are generated, which can cause computational burden. Therefore, in this study, each converter has independent control, divided as follows: rectifier control, DAB control, and inverter control.

A. Rectifier Control

The rectifier stage of the SST is typically connected to medium or high voltage. To connect medium voltage converters, the most common solution found in the literature is to connect converters in series. As the voltage increases, more converters need to be connected in series, resulting in a larger number of possible combinations of switch states.

To minimize the computational burden caused by many converters connected in series, several studies were conducted on sectorization of the multilevel converter. This strategy consists in dividing the converter into smaller parts, which significantly reduces the number of possibilities that the control must evaluate [15][16].

In this study, two converters connected in series allowed the rectifier to operate at the MVAC bus voltage. The Finite Set Model Predictive Control (FS-MPC) was used, which applies

one optimal switching state found by minimizing a performance-dependent cost function and uses a discrete model to anticipate future system states [17].

This control aims to ensure a constant MVDC bus voltage and help regulate the public grid voltage (MVAC bus) by injecting or consuming reactive power.

The first step is to define the current that the rectifier needs to synthesize. The current was calculated using the pq theory [18]. To calculate the direct axis component i_α^* and quadrature component i_β^* of the current that the converter needs to synthesize, the values of the direct and quadrature voltage components v_α and v_β, desired active power P^*, and desired reactive power Q^* are required.

The reactive power control helps regulate the voltage of the public grid by comparing the desired voltage $|v_{MVAC}^*|$ with the measured voltage value. The direct and quadrature voltage positive sequence components v_α and v_β of v_{MVAC} are dynamically extracted from the grid voltage using a Second Order Generalized Integrator (SOGI) with a Frequency Locked Loop (FLL). Due to the single-phase nature of the circuit, the v_β component is fictitious and is obtained by a quarter-cycle delay of the v_α voltage signal [19]. In this case, $v_\alpha = v_{MVAC}$. After the direct axis and quadrature components are measured voltage, they are used to calculate the magnitude of $|v_{\alpha\beta}|$ using (18).

$$|v_{\alpha\beta}| = \sqrt{v_\alpha^2 + v_\beta^2} \tag{18}$$

The error between $|v_{MVAC}^*|$ and $|v_{\alpha\beta}|$ values goes into a PI controller to generate the required amount of reactive power Q^* to adjust the voltage on the MVAC bus.

The MVDC voltage control is performed by comparing the measured values of V_{MVDC1} and V_{MVDC2} with the desired value V_{MVDC}^*. The error between these values is used as the input to the PI controller. The total active power P^* required from the rectifier to regulate each DC-link voltage is determined from the PI output signals. Fig. 5 shows the reference signals of the main control loop. Since the i_β component is fictitious, $i_\alpha^* = i_r^*$.

The optimal switching state is determined by minimizing the cost function, which involves comparing the desired values with the 16 predicted values from the MPC. The cost function is defined by (19).

$$G_R = w_r \cdot (i_r^* - i_r^N)^2 + w_{dc} \cdot (V_{MVDC1}^* - V_{MVDC1}^N)^2 + w_{dc} \cdot (V_{MVDC2}^* - V_{MVDC2}^N)^2 + w_v \cdot (V_{MVDC1}^N - V_{MVDC2}^N)^2 \tag{19}$$

Where $w_r = 1$, $w_{dc} = 1$, and $w_v = 2$ are the weights assigned to the input current, output voltage, and DC-link balance voltages.

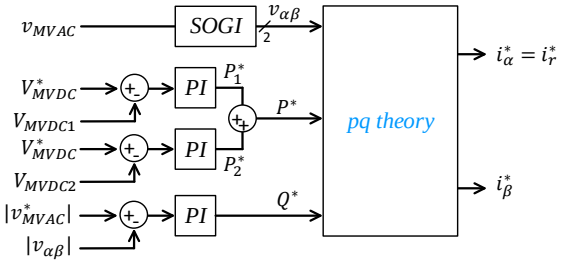

Fig. 5. Reference signals main loop control.

Fig. 6 shows an overview of the predictive control model and power circuit of the rectifier.

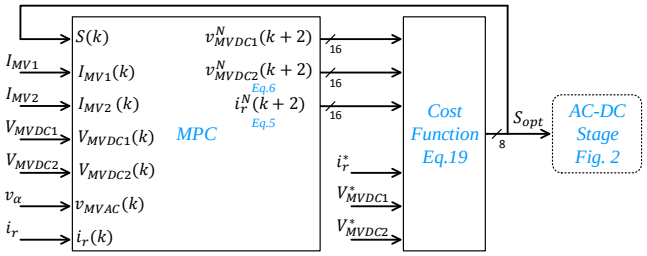

Fig. 6. MPC Rectifier control overview.

B. DAB Control

In this study, the DAB converter will be powered by the rectifier. Thus, the main goal of the control system is to control the LVDC voltage supplying various types of loads.

The adopted strategy is based on the master-slave concept, where one converter regulates the voltage on the LVDC bus, while the other converters inject current using the criteria presented in (11). This study employs six DAB converters (two per phase). Each DAB converter is controlled separately, thus each one has its own control system.

The voltage on the LVDC bus is controlled by the first converter ($m = 1$) using Model Predictive Control. This method involves selecting three angles based on the last angle used in control [20] [21], as shown in Equation (20).

$$\delta_{set} = \left[(\delta_{old} - \delta_{step});\ \delta_{old}\ ;\ (\delta_{old} + \delta_{step})\right] \tag{20}$$

Where δ_{old} is the phase shift applied at the previous instant, and δ_{step} is dynamically evaluated according to (21) to increase or decrease the transferred power.

$$\delta_{step} = \delta_{min} \cdot (1 + \alpha \cdot V_{adp}) \tag{21}$$

Where,

$$V_{adp} = \begin{cases} |V_{LVDC}^* - V_{LVDC}|; & if\ |V_{LVDC}^* - V_{LVDC}| \le V_T \\ V_T; & if\ |V_{LVDC}^* - V_{LVDC}| > V_T \end{cases} \tag{22}$$

Where V_{LVDC}^* is the desired output voltage of the DAB converter, α is a gain, δ_{min} is the lowest phase shift angle, and V_T is the maximum value for V_{adp}.

The three possible values of δ_{set} are used to calculate the output voltage. According to the cost function (23), the one that presents the smallest error compared to the reference value is chosen [20] [21].

$$G_{DABv} = \alpha_1 \cdot \left(V^*_{LVDC} - V_{LVDC}(k+2)\right)^2 + \alpha_2 \cdot \left(I^N_{0DC1}(k+1) - I_{01}(k)\right)^2 \quad (23)$$

Where α_1 and α_2 are gains adjusted according to the method presented in [22], and their values are $\alpha_1 = 1$ and $\alpha_2 = 1$.

Fig. 7 shows an overview of the predictive control model for the output voltage and power circuit of the DAB, where δ_{opt} represents the optimal phase shift. The DAB converter switches are triggered by the SPS Control block, which is based on the phase shift delivered by the cost function.

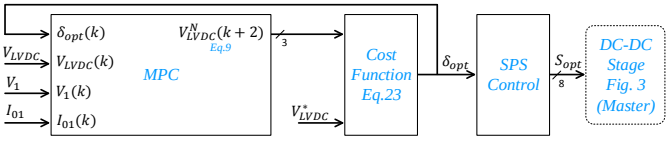

Fig. 7. DAB Converter Control (m=1): Voltage control overview.

The converters $m = 2, 3, \ldots, 6$ are controlled to ensure that all six DAB converters transfer the same amount of power. The current of converter $m = 1$, which controls the LVDC's voltage, is used as the reference current. The error between this current and the output current of the m^{th} converter is fed into the PI controller to generate a reference power P^*_{ref}. Similar to the voltage controller, this control method uses three phase-shifts (20) to predict the three possible power outputs P^N_m for the next cycle. The cost function (24) defines the optimal phase-shift to balance the currents between the converters.

$$G_{DABi} = \alpha_1 \cdot \left(P^*_{ref} - P_{DABJ}(k+1)\right)^2 + \alpha_2 \cdot \left(P_{DABJ}(k+1) - P_{DABJ}(k)\right)^2 \quad (24)$$

Fig. 8 shows an overview of the predictive control model output current and power circuit of the DAB.

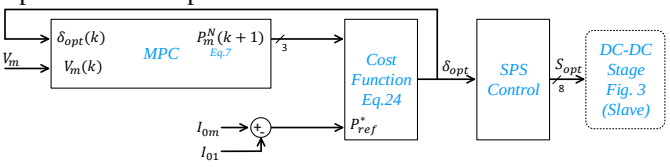

Fig. 8. DAB Converter Control (m=2, 3, … ,6): Current control overview.

C. Inverter Control

The FCS-MPC technique was used in VSI control in many studies due to its simple implementation and online optimization [23][24].

This control method aims to generate three-phase voltages at the LVAC bus. Thus, the voltage in the output capacitor must follow the reference three-phase voltages v^*_{LVAC}. The delay in reference tracking in predictive control schemes [25] affects the control system.

One way to reduce reference tracking delay in predictive control schemes is to apply extrapolation methods. For sinusoidal references and large sampling times, LaGrange extrapolation can generate future references using only present and past values of the current reference [25]. Equation (25) shows how to calculate the reference in the stationary $\alpha\beta$ frame $\boldsymbol{V^*_{\alpha\beta}}(k+2)$.

$$\boldsymbol{V^*_{\alpha\beta}}(k+2) = 6 \cdot \boldsymbol{V^*_{\alpha\beta}}(k) - 8 \cdot \boldsymbol{V^*_{\alpha\beta}}(k-1) + 3 \cdot \boldsymbol{V^*_{\alpha\beta}}(k-2) \quad (25)$$

The cost function is presented in (26), and its value is calculated based on the squared difference between the reference value and predicted values. The switching set that results in the lowest value of the cost function will be selected.

$$G_I = \left(\boldsymbol{V^*_{\alpha\beta}}(k+2) - \mathbf{V^P_{C\alpha\beta}}(k+2)\right)^2 \quad (26)$$

Fig. 9 shows an overview of the predictive control model used in LC-filter VSI.

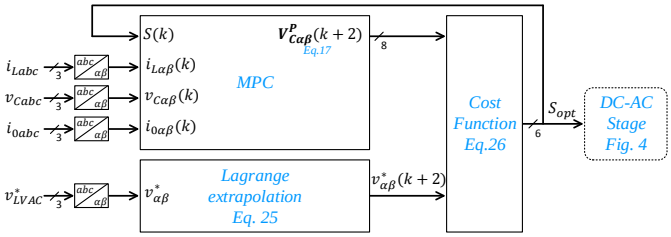

Fig. 9. MPC VSI control overview.

IV. Results

The results were obtained by real-time simulation in OPAL OP5700 (RCP/HIL Virtex7 FPGA-based Real-Time Simulator) using the three-phase SST topology (Fig. 1). Each module was controlled by its respective Model Predictive Control, which was previously presented. Table 1 presents the most important parameters used in simulation.

TABLE I
Main Parameters

Parameter	Symbol	Value
$MVAC$ rated Voltage	v_{MVAC}	$2200V$
$MVDC$ rated Voltage	V_{MVDC}	$1000V$
$LVDC$ rated Voltage	V_{LVDC}	$500V$
$LVAC$ rated Voltage	v_{LVAC}	$220V$
Grid frequency	f	$50Hz$
Sample Time	T_s	$50\mu s$
Switching Frequency	f_{sw}	20kHz
SST rated Power	P	$300kW$
RL Filter (AC-DC)	l_{MV}	$15m$H
	r_{MV}	$10m\Omega$
Capacitor (AC-DC)	C_r	$40m$F
Inductor (DC-DC)	$L_{k1,2,\ldots,6}$	31.25μH
Capacitor (DC-DC)	$C_{01,2,\ldots,6}$	$15.6m$F
LC Filter (DC-AC)	L_f	500μH
	C_f	670μF

Seven scenarios were analyzed to demonstrate the SST's ability to reject grid disturbances. In the first scenario, a linear

load with a power factor of 0.8 (inductive) was connected to the LVAC grid. Fig. 10(a) shows the results indicating that the power factor at the MVAC is unity and that the SST can effectively act as a reactive compensator for the LVAC side. In the second scenario, a nonlinear load was connected to the LVAC grid. Fig. 10(b) shows that, regardless of the non-sinusoidal LVAC current, the current in the MVAC grid remained sinusoidal. The SST acted as a harmonic compensator for the MVAC side.

In the third scenario, renewable energy sources are integrated into the LVDC grid, and a $60\,kW$ power step is injected into the DC grid. Fig. 11(a) shows the behavior of the SST in this scenario, in which the voltage in the MVDC bus experiences a brief transient of approximately $150\,ms$. In the fourth scenario, the effect of a power step ranging from $0\,kW$ to $40\,kW$ is evaluated, simulating, for example, an electric vehicle fast charging station. Fig. 11(b) shows the behavior of the SST in this scenario. The transient is determined after $100\,ms$ in the MVDC bus. In both experiments, there are no changes on the LV side.

Fig. 12(a) and Fig. 12(b) show the response of the SST when a three-phase and single-phase fault, respectively, causes a voltage drop of $0.7\,pu$ on the MVAC grid for $300\,ms$. In these two scenarios, the voltage drops results in an increase in MVAC current. However, in both cases, the issue in the MVAC bus does not affect the LV side.

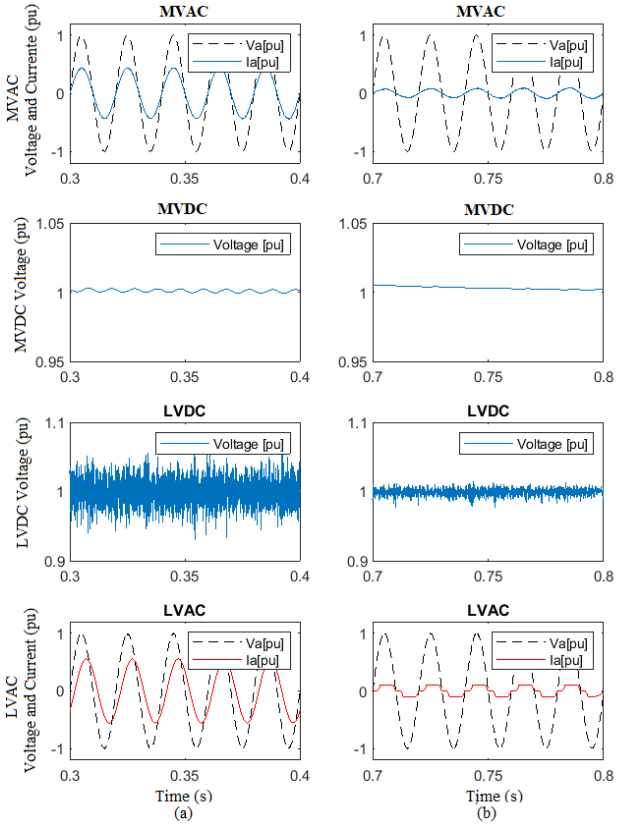

Fig. 10. The SST rejection of grid disturbances. (a) Power Factor Compensation. (b) A nonlinear load on the LV grid.

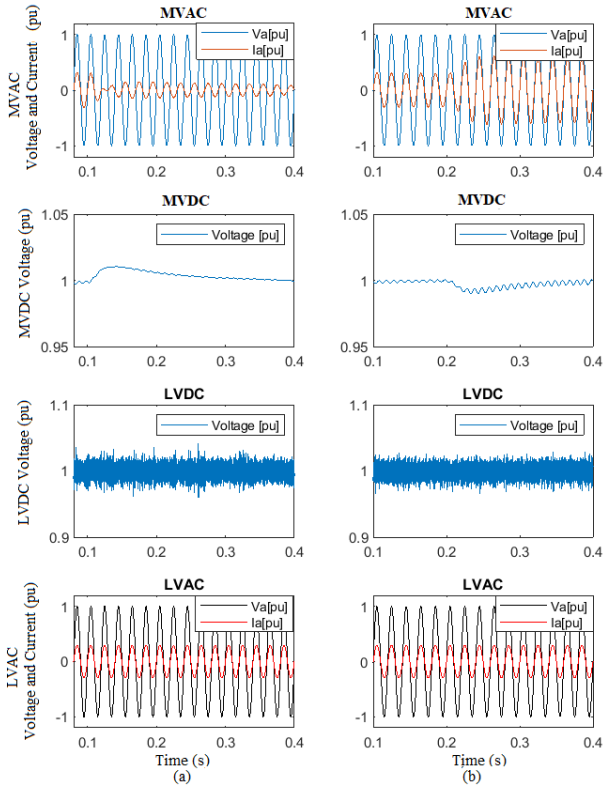

Fig. 11. The SST rejection of grid disturbances. (a) A renewable power injection on the LVDC side. (b) The power step change in an EV fast-charging station on the LVDC side.

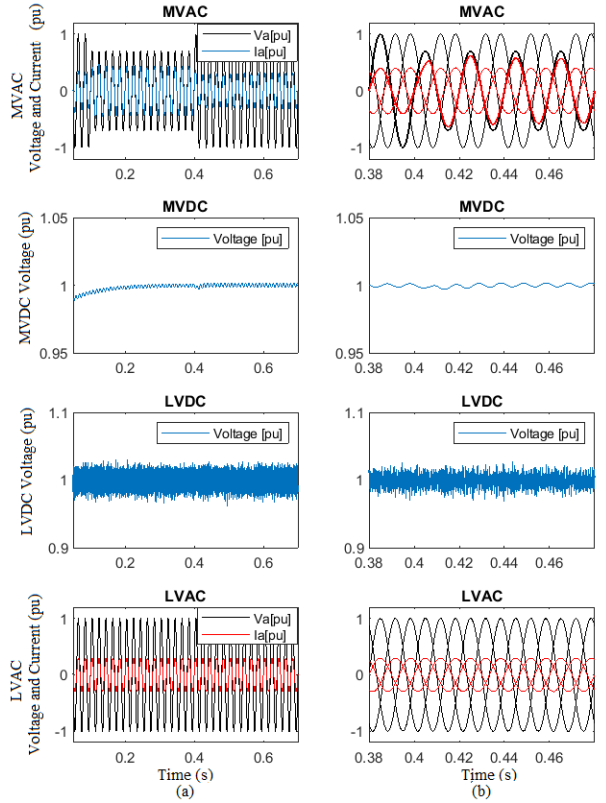

Fig. 12. The SST rejection of grid disturbances. (a) The voltage sag following a three-phase fault in the MVAC grid. (d) The voltage sag following a single-phase fault in the MVAC grid.

Finally, the last experiment aims to demonstrate the SST's ability to assist in regulating the voltage on the MVAC bus by injecting or consuming reactive power. Fig. 13 shows a scenario in which the voltage on the MVAC bus decreases and then increases due to factors such as instabilities in the generation system or high impedances in the power distribution line. Fig. 13(a) shows the behavior of the MVAC bus without reactive power control, while Fig. 13(b) shows the behavior with reactive power control. In this scenario, the voltage on the MVAC bus remains constant, unlike what is shown in Fig. 13(a).

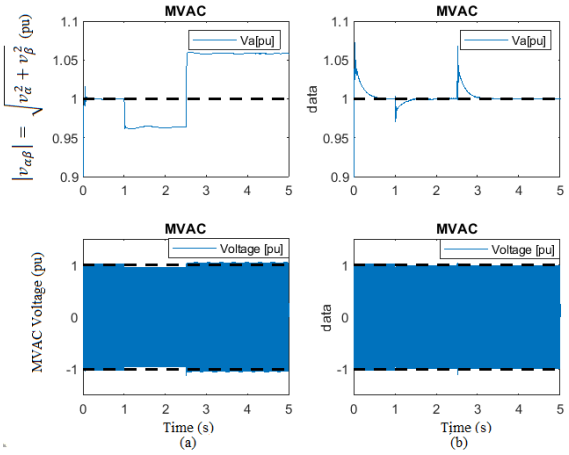

Fig. 13. Assistance in adjusting the MVAC grid (a) without compensation (b) with compensation.

V. Conclusions

This study demonstrates the effectiveness of using model predictive control (MPC) to control a complete three-stage SST structure in a modular way, demonstrating that the computational effort, in this case, is not related to the size of the SST. Real-time simulation results showcase its features, including reactive power compensation and grid disturbance rejection. The bidirectionality of the SST is also demonstrated by the application of renewable energy sources to the LVDC bus. Moreover, grid disturbance rejection is analyzed by the single-phase and three-phase voltage sag of $0.7\,pu$ on the MVAC side, showing that the LVDC and LVAC buses continue to function perfectly.

VI. References

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