A Computationally Efficient Approach for Power Semiconductor Loss Estimation of Modular Multilevel Converters in EMT Simulations

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Abstract— **This paper presents a computationally efficient approach for estimating the power semiconductor losses of a modular multilevel converter (MMC) in electromagnetic transient (EMT) simulations. Earlier approaches required the loss estimation to be carried out at the individual IGBT-diode component level. In contrast, this paper extends this concept to the simulation of an entire MMC arm thus speeding up the simulation significantly. The proposed approach can accurately estimate the losses during steady state as well as transient operation with great speed. Furthermore, the loss estimates of each individual submodule can also be reported separately with the proposed approach, if needed. It is verified using a simulation test case of a two-terminal MMC-HVdc link and comparing the computed losses against the earlier (but much slower) approach of computing the losses at individual switch level.**

Keywords: **Electromagnetic Transient (EMT) Simulations, Modular Multilevel Converters (MMC), Power Loss**

I. INTRODUCTION

MODULAR multilevel converter (MMC) is a popular voltage source converter (VSC) topology commonly used for medium and high voltage applications due to its flexibility, scalability, modularity, and superior harmonic performance [1]. Each phase leg of an MMC consists of an upper and lower arm (as shown in Fig. 1), each of which contains stacks of series-connected submodules (SM) for generating a stepped waveform that closely resembles a sinusoidal wave [2]. Typical SMs comprise of power semiconductor switches (IGBT-diode pairs) and a capacitor as illustrated in Fig. 2. Power loss occurs in these switches in the ON state (i.e., conduction loss), the OFF state (i.e., blocking loss) and while transitioning between the ON and OFF state (i.e., switching loss). An accurate quantification of these losses under all operating scenarios (steady-state as well as transient) is essential to ensure that the switches always operate within their limits as well as for effectively designing their thermal management system [3].

For high-power applications, it is generally not feasible to evaluate these power losses experimentally [4]. Hence, one has to resort to analytical or simulation-based techniques for effectively estimating them. Several analytical approaches for loss estimation of MMCs have been proposed in the literature [5]–[8]. However, these approaches make a lot of simplifying assumptions and typically are not able to quantify the impact of a converter's controls on its power losses [4].
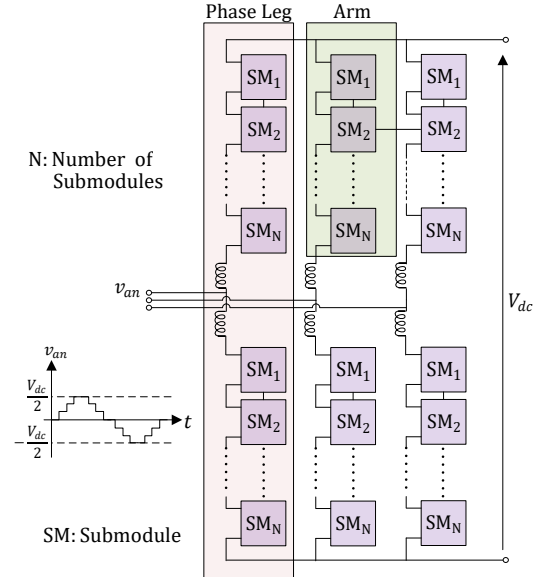

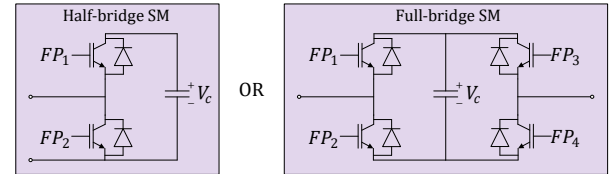Fig. 1. Modular Multilevel Converter (MMC)

Fig. 2. Typical MMC Submodules

On the other hand, simulation-based approaches can estimate the losses under a wide range of operating scenarios (steady-state as well as transient). Additionally, the impact of a converter's controls on its power losses can also be studied [2], [4]. This makes such approaches an attractive option for estimating the power losses of MMCs. Several simulation-based approaches have been proposed in the literature for estimating the losses of VSCs [9]–[13]. However, these approaches generally require device-level voltage and current information for estimating the losses. If applied directly for estimating the losses of an entire MMC, these methods can make the simulation computationally burdensome. This is because each switch in an MMC would need to be modelled individually in order to obtain the required device-level information. This increases the number of nodes in the simulated circuit, thereby significantly increasing the

computational burden.

Modern electromagnetic transient (EMT) simulation programs typically combine an entire MMC arm into a single equivalent whose parameters in each time-step are calculated from the individual firing pulses and the initial conditions at the beginning of the time-step [14]. This approach can improve the simulation time significantly [14]. However, as the switches are not individually modelled, it is not possible to directly apply the loss estimation procedures that require device-level information (e.g., [9]–[13]).

In this paper we present a computationally efficient approach for estimating the power losses of MMCs in EMT simulations. The loss estimation is carried out using an arm-level detailed equivalent model (DEM) [14] of an MMC, thereby speeding up the overall simulation significantly. The approach proposed in [13] is utilized in this paper for estimating the power semiconductor losses. The device-level information required for this approach is obtained by coalescing the algorithm used for updating the DEM in every simulation time-step with the loss estimation approach of [13]. Note that even though an arm-level equivalent is utilized, the losses are not just estimated for the entire arm; the proposed approach also allows for reporting the loss estimates of each individual MMC submodule separately, if needed. In order to make sure that the MMC's losses are accurately evaluated during steady state operation as well as transient conditions, an enhanced DEM [15], [16] of MMC is utilized.

The paper begins with a brief discussion of the simulation-based loss estimation approach proposed in [13]. Then, a brief review of the DEM [14]–[16] of an MMC is presented. The proposed approach for efficiently estimating the losses of an MMC is presented in detail after this. Finally, a simulation test case of a two-terminal MMC-based HVdc link is used for benchmarking the accuracy and computational efficiency of the proposed approach. Although the approach in this paper is discussed for an MMC that uses half-bridge SMs, it can be easily extended to other SM topologies as well.

II. SEMICONDUCTOR POWER LOSS ESTIMATION IN EMT SIMULATIONS

A. Losses in Power Semiconductor Switches

Losses in power semiconductor switches can be categorized as: (i) conduction loss, (ii) blocking loss, and (iii) switching loss. Conduction loss can be easily evaluated in an EMT simulation by multiplying the device's ON state current with its ON-state voltage drop. Similarly, blocking loss can be evaluated by multiplying the OFF-state voltage across the device with its OFF-state leakage current. The challenge lies in estimating the switching loss. EMT simulators usually model a semiconductor switch using a bivalued ON/OFF resistor [3]. However, such a simplified model by itself is not sufficient for estimating the switching loss.

B. Switching Loss Estimation in EMT Simulations

Switching loss in an IGBT-diode pair (such as the one used in MMCs – see Fig. 2) mainly consist of turn-on and turn-off losses of the IGBT as well as the reverse recovery loss of the freewheeling diode [3]. A device-level simulation model [17]

of a power semiconductor switch can certainly be used for estimating its switching loss. However, such models require the use of a very small time-step (in the range of nanoseconds) for accurately capturing the switching phenomena [3]. It is generally not feasible to use such small time-steps in system-level EMT simulations (that typically use time-steps in the microsecond range) without significantly increasing the computational burden.

(a) Approximated IGBT turn-on waveform

(b) Approximated IGBT turn-off waveform

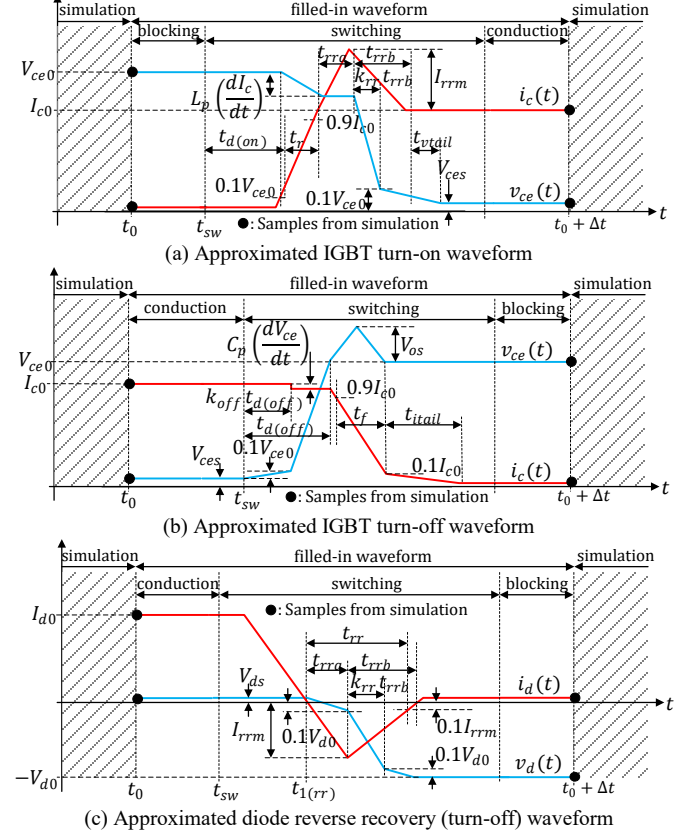(c) Approximated diode reverse recovery (turn-off) waveform
Fig. 3. Piecewise linear switching waveforms used in the approach of [13]

Reference [13] proposes an EMT simulation-based loss estimation approach that is not only accurate but also computationally efficient and simple to implement. In this approach, a device-level switch model is NOT used in the network simulation of an EMT simulation; instead, the network solution is still computed using the bivalued ON/OFF resistor model for the switches. Then, physics-based piecewise linear approximations for the waveforms of the device voltage and current (as shown in Fig. 3[1]) are obtained from the (larger time-step) EMT simulation using the following:

(a) the pre- and post-switching device voltages and currents, which can be obtained from the network solution of the EMT simulation,

(b) the precise time of switching (t_{sw}) for the devices which can be obtained from EMT simulations that support interpolated switching [18], [19], and

(c) the information about the device's switching performance, which can be obtained from physical tests or from its datasheet.

These waveforms are then multiplied and averaged to yield

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[1]The switching duration has been deliberately magnified compared to the simulation time-step Δt for making the illustration clearer.

the switching loss in that time-step. The time-step can be several times larger than the switching interval (although it must be sufficiently small to capture each individual switching as a separate event) [3], [13]. As the estimated waveforms adhere to the physics of the switching process, they can be used for estimating the switching loss [3]. The detailed equations used for computing the switching loss using the estimated waveforms shown in Fig. 3 are given in [13]. As the device representation in the network solution is still the simple ON/OFF resistor type, the incremental computational burden of this approach is very marginal [3], [13].

A number of parameters associated with the switching performance of a semiconductor device are required for obtaining the approximated switching waveforms (as in Fig. 3) in the approach of [13]. These are given in Table 1 for the Toshiba ST1500GXH24 IGBT-diode power module [20] rated at 4.5 kV, 1.5 kA (same as the one used in [2]). Information on how to obtain these parameters can be found in [3], [4], [13].

TABLE 1.
Device parameters required for the approach of [13]
(Toshiba ST1500GXH24 IGBT-diode module [20])

Parameter	Nominal Values
IGBT on-state saturation voltage (V_{ces})	3.0 V
Turn-on delay ($t_{d(on)}$) and rise time (t_r)	700.0 ns, 500.0 ns
Turn-on voltage tail time (t_{vtail})	2500.0 ns
Turn-off delay ($t_{d(off)}$) and falling time (t_f)	7500.0 ns, 2000.0 ns
Turn-off voltage rise delay factor (k_{off})	0.95
Turn-off current tail time (t_{itail})	2000.0 ns
Diode on-state saturation voltage (V_{ds})	3.2 V
Diode reverse recovery time (t_{rr})	1000.0 ns
Diode reverse recovery time ratio (k_{rr})	0.4
Diode peak reverse recovery current (I_{rrm})	1.75 kA
Stray inductance (L_p) and capacitance (C_p)	330 nH, 5.0 nF

Using the estimated losses and known ambient conditions, the junction temperature of each device can also be determined. In this paper, this is done using the method proposed in [3], which solves a heat flow problem where the thermal model of the IGBT-diode module and the heat sink is represented by a lumped parameter equivalent circuit. This process is schematically illustrated in Fig. 4. The details about this can be found in [3] and are not discussed here for the sake of brevity.
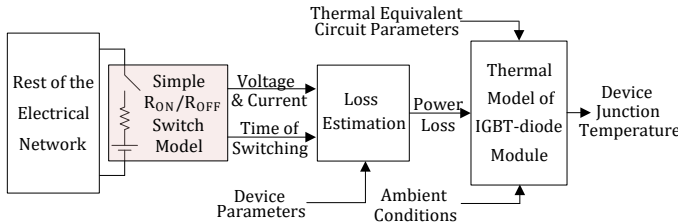

Fig. 4. Schematic illustration of the approach for device loss estimation and junction temperature calculation

III. DETAILED EQUIVALENT MODEL OF MMC

A. Basic Detailed Equivalent Model (DEM)

As seen in Fig. 1, MMCs employ a large number of power semiconductor switches to facilitate the required power conversion (AC to DC or vice versa). While simulating an MMC in an EMT simulator, if each of these switches is modelled explicitly, then the simulation can become computationally onerous. To overcome this bottleneck, a detailed equivalent model (DEM) of an MMC has been proposed in the literature [14].

In this technique, firstly knowing the values of the firing pulses for each switch as well as the initial conditions at the beginning of a time-step, an SM is replaced with its Thevenin equivalent. This is possible because in an EMT simulation, the switches are typically modelled as bivalued ON/OFF resistors and the capacitor is modelled using its discrete-time companion circuit equivalent [21]. Now, as all the SMs in each MMC arm are series-connected, the entire arm can be combined into a single Thevenin equivalent (as shown in Fig. 5). This reduced-order equivalent is then utilized for computing the network solution of an EMT simulation. This drastically reduces the number of nodes in the simulated circuit, and hence makes the simulation computationally efficient [14].
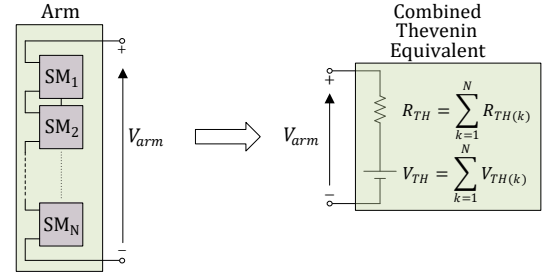

Fig. 5. Reduced order equivalent for an MMC arm in an EMT simulation

Although this "basic" DEM technique is efficient, [15], [16] have shown that it is accurate only under steady-state operating conditions and fails to accurately model an MMC's behavior when it is completely blocked (i.e., when gate pulses to all SM switches are 0). To remedy this, [15], [16] propose an "enhanced" DEM. This technique is briefly discussed here for the half-bridge SM case.

B. Special Considerations for Accurately Modelling Complete Blocking of the MMC bridge

During startup as well as following a dc side fault, typically an MMC is completely blocked (i.e., each SM's IGBTs are NOT issued any gate pulses). In this case, although the IGBTs are off, their anti-parallel diodes can still conduct depending on the direction of the arm current i_{arm} (as shown in Fig. 6). Additionally, these diodes can change their conduction state depending on the direction of i_{arm}. A change in the direction of i_{arm} can happen at any time (need not be at an integral multiple of the time-step). However, with the "basic" DEM of [14], these changes get constrained to occur at the integral multiples of the time-step in a fixed time-step EMT simulator, which can cause significant inaccuracies [15], [16].

References [15], [16] propose an "enhanced" DEM for remedying this situation. The arm-level equivalent circuit for this approach for an MMC comprising of half-bridge SMs is as shown in Fig. 7. In this, the basic DEM obtained from internal node collapsing using the approach of [14] (shown in the red dotted box in Fig. 7) is augmented with two extra IGBTs (T_{eq1} and T_{eq2}) and a diode (D_{eq1}). These extra switching elements must support interpolated switching [18],

[19] in a fixed time-step EMT simulator so that the transitions in between time-steps between the scenarios shown in Fig. 6 can be modelled accurately [16].
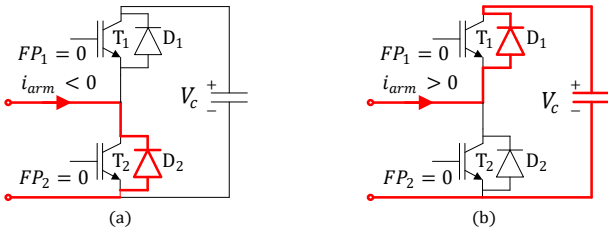

Fig. 6. Half-bridge SM - Possible conduction paths when completely blocked
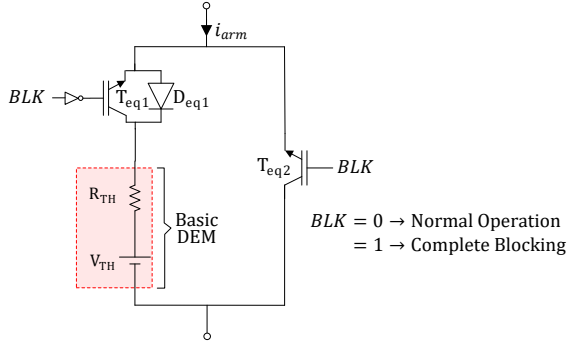

Fig. 7. Enhanced DEM for a half-bridge SM-based MMC

IV. EFFICIENTLY ESTIMATING THE POWER LOSS OF MMC

The approach proposed in [13] has been shown to provide reliable loss estimates through EMT simulations for various voltage source converter topologies, including the MMC [2], [4], [13]. However, as discussed in Section II, it requires device-level information obtained from the network solution of an EMT simulation for estimating the losses. If this approach is used directly for estimating the losses of an entire MMC, it would require modelling each switch in an MMC individually for obtaining the required device-level information. This increases the number of nodes in the simulated circuit and thus makes it computationally burdensome. An arm-level DEM of an MMC has been shown to significantly improve the computational efficiency of an EMT simulation [14]–[16]. However, the device-level information required for the loss estimation is not directly available in this case as all internal nodes of an MMC arm are eliminated. Thus, directly applying the loss estimation approach of [13] with a DEM is not possible.

Based on the discussion in Section III, we know that the parameters R_{TH} and V_{TH} of a DEM (seen in Fig. 7) can change in every simulation time-step and are determined by knowing the following at the beginning of each time-step: (i) the firing pulses for each switch, which come from the converter's controls, and (ii) the initial conditions. These initial conditions are each SM's node voltages and branch currents, which are computed in every time-step internally while updating the arm-level DEM. Knowledge of these initial conditions along with the ON/OFF status of each switch and the device parameters (like those given in Table 1) is sufficient to obtain the approximated switching waveforms (as given in Fig. 3) and thereby estimating the power loss.

Thus, a computationally efficient way of estimating the power semiconductor losses of an MMC is by coalescing the loss-estimation approach of [13] with the algorithm used for deriving the DEM in every time-step, as illustrated in Fig. 8. As this approach utilizes the DEM, it estimates the losses of an MMC without penalizing the computational efficiency of the simulation. The details of how the loss estimation can be carried out using each SM's initial conditions as well as the ON/OFF status of the switches is illustrated in the flowchart[2] of Fig. 8. To ensure that MMC's losses are accurately evaluated during normal operation as well as when it is completely blocked, the enhanced DEM [15], [16] discussed in Section III.B is utilized and the flowchart shown in Fig. 8 is also divided accordingly (i.e., one part (blue) that estimates the losses under normal operation whereas the other part (red) that estimates them when the MMC is completely blocked). The nomenclature used for the different switching elements (i.e., IGBTs, diodes) and the firing pulse signals (FP$_1$, FP$_2$) in the flowchart of Fig. 8 is based on that in Fig. 6 and Fig. 7. Note that as seen from Fig. 8, the loss estimates of each individual submodule are separately computed and can be made available to the user, if required.

A. Obtaining the required device-level information

As discussed in Section II.B, the approach of [13] requires two pieces of device-level information from the network solution of an EMT simulation in each time-step to estimate the power losses. These are: (i) the pre- and post-switching device voltages and currents, and (ii) the time of switching (t_{sw}) for the devices. The prior can be obtained from the internal node voltages and branch currents computed for each SM when the DEM is updated at the beginning of each simulation time-step, while the latter can be obtained in the case of a DEM, as explained below:

Normal Operation (BLK = 0):

In the enhanced DEM of Fig. 7, during normal operation the IGBT T$_{eq2}$ is always OFF (as $BLK = 0$) whereas the IGBT T$_{eq1}$ and the diode D$_{eq1}$ conduct based on the direction of the arm current i_{arm}. Therefore, the arm-level equivalent circuit is the same as the basic DEM given in Fig. 5.

In the case of the basic DEM, by knowing the values of the firing pulses of each SM's switches at the present and the previous time-step as well as the direction of i_{arm}, the status of these switches at the present time-step can be accurately inferred. Then using these as well as the known status of the switches at the previous time-step, the time of switching (t_{sw}) for each SM's switches can be computed.

Complete Blocking Scenario (i.e., BLK = 1):

When the MMC bridge is completely blocked, each SM can be in either one of the states that are shown in Fig. 6. Moreover, the transition between these two states can happen at any time. This fact is modelled accurately in the enhanced DEM of Fig. 7 by having the extra IGBTs (Teq1 and Teq2) and diode (Deq1) support interpolated switching [18], [19]. Additionally, IGBT Teq1 is always OFF (as $BLK = 1$) whereas the IGBT Teq2 and the diode Deq1 conduct based on the direction of the arm current i_{arm}.

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[2]The proposed approach is discussed here for an MMC that uses half-bridge SMs. However, it can be easily extended to any other SM topology.

Top flowchart (process):

Start → Set i = 1 → [i ≤ N ?]

N: Number of Submodules

[i ≤ N ?] — Yes → Compute the initial conditions (node voltages & branch currents) of ith SM → Estimate the losses of ith SM → Compute the contribution of ith SM to the DEM → i = i + 1 → (loops back)

[i ≤ N ?] — No →
- Add DEM to Admittance Matrix & RHS Vector of EMT Simulation's Network Solution
- Add the computed losses to total losses.
→ End

Detailed flowchart (Estimate the losses of ith SM):

Start → [BLK(t) = 1?]

[BLK(t) = 1?] — Yes → **Complete Blocking Scenario**

[D_{eq1} ON at t?]
- Yes → [D_{eq1} ON at $(t - \Delta t)$?]
  - Yes → Diode D_1 conducting. Compute:
    - Conduction Loss of D_1
    - Blocking Loss of D_2, T_1 & T_2
  - No → Diode D_1 switched ON, Diode D_2 switched OFF. Compute:
    - Reverse Recovery Loss of D_2
    - Blocking Loss of T_1 & T_2
- No → [D_{eq1} ON at $(t - \Delta t)$?]
  - Yes → Diode D_2 switched ON, Diode D_1 switched OFF. Compute:
    - Reverse Recovery Loss of D_1
    - Blocking Loss of T_1 & T_2
  - No → Diode D_2 conducting. Compute:
    - Conduction Loss of D_2
    - Blocking Loss of D_1, T_1 &

[BLK(t) = 1?] — No → **Normal Operation**

[$i_{arm}(t) \geq 0$?]
- No → [$FP_2(t) = 1$?]
  - Yes → [$FP_2(t - \Delta t) = 1$?]
    - No → IGBT T_2 conducting. Compute:
      - Conduction Loss of T_2
      - Blocking Loss of D_1, D_2 & T_1
    - (Yes path above) IGBT T_2 switched ON, Diode D_1 switched OFF. Compute:
      - Turn-on Loss of T_2
      - Reverse Recovery Loss of D_1
      - Blocking Loss of T_1 & D_2
  - No → [$FP_2(t - \Delta t) = 1$?]
    - Yes → IGBT T_2 switched OFF, Diode D_1 switched ON. Compute:
      - Turn-off Loss of T_2
      - Blocking Loss of T_1 & D_2
    - No → Diode D_1 conducting. Compute:
      - Conduction Loss of D_1
      - Blocking Loss of T_1, T_2 & D_2
- Yes → [$FP_1(t) = 1$?]
  - Yes → [$FP_1(t - \Delta t) = 1$?]
    - No → IGBT T_1 conducting. Compute:
      - Conduction Loss of T_1
      - Blocking Loss of D_1, D_2 & T_2
    - Yes → IGBT T_1 switched ON, Diode D_2 switched OFF. Compute:
      - Turn-on Loss of T_1
      - Reverse Recovery Loss of D_2
      - Blocking Loss of T_2 & D_1
  - No → [$FP_1(t - \Delta t) = 1$?]
    - Yes → IGBT T_1 switched OFF, Diode D_2 switched ON. Compute:
      - Turn-off Loss of T_1
      - Blocking Loss of T_2 & D_1
    - No → Diode D_2 conducting. Compute:
      - Conduction Loss of D_2
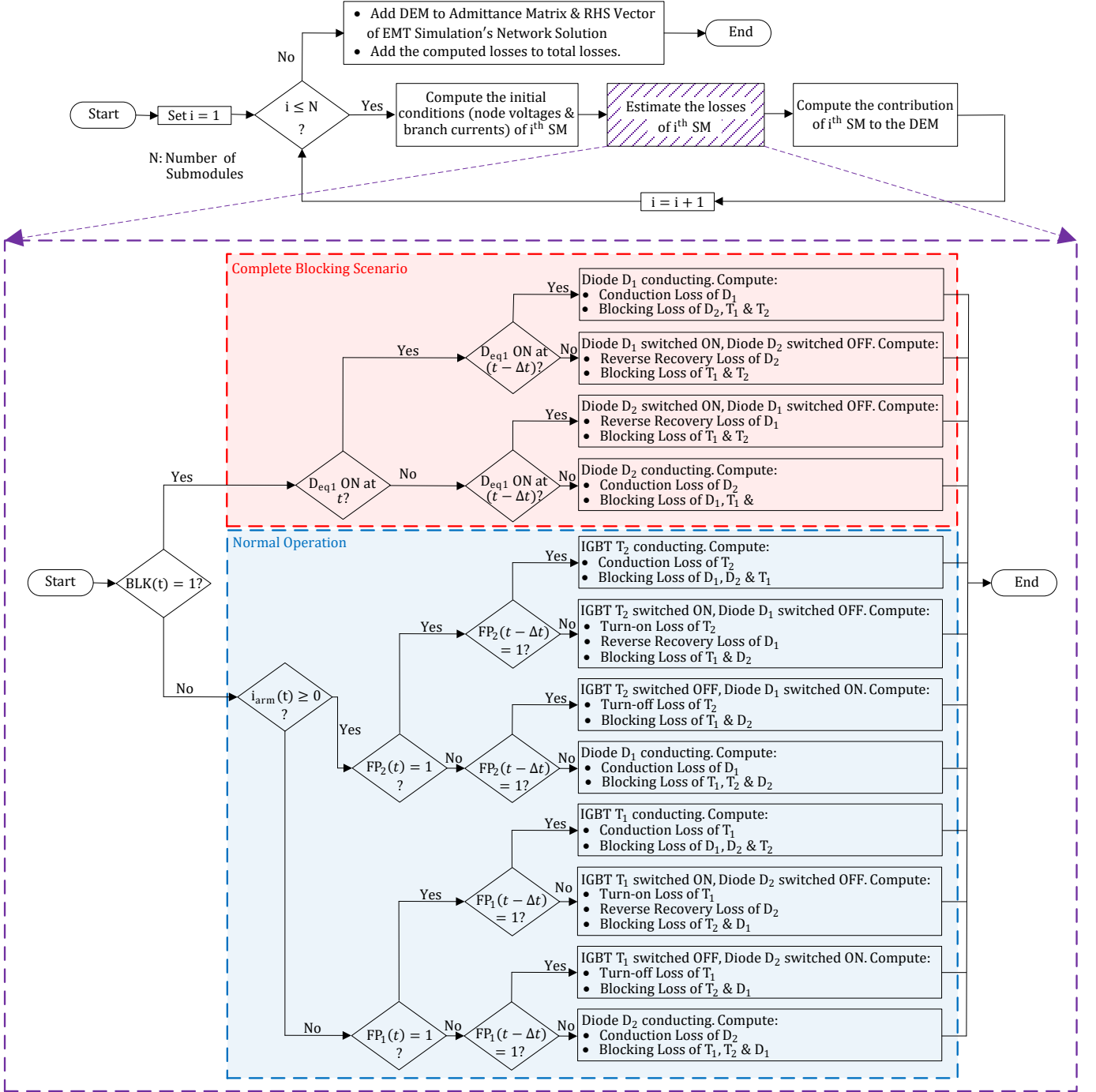   - Blocking Loss of T_1, T_2 & D_1

→ End

Fig. 8. The proposed approach for efficiently estimating the power semiconductor losses of an MMC comprising of half-bridge SMs

When Deq1 conducts, the behavior shown in Fig. 6 (a) is modelled whereas when Teq2 conducts, the behavior shown in Fig. 6 (b) is modelled for the overall MMC arm. Therefore, using the switching times of Deq1 and Teq2, the precise times of switching can be obtained for each SM's diodes D1 and D2, respectively under the complete blocking scenario.

V. VALIDATION TEST CASE

In order to validate the proposed approach, we consider a simulation test case consisting of a two-terminal MMC-HVdc link as shown in Fig. 9. The system is rated at 180 MW, ± 75 kV and the converters at each end have 50 half-bridge SMs per arm with a nominal SM voltage of 3 kV. Both ends are interconnected using two 200 km overhead transmission lines which are modelled using the frequency dependent model [22]. The IGBT-diode module used in each SM of the MMC bridges is assumed to be the Toshiba ST1500GXH24 [20] rated at 4.5 kV, 1.5 kA (same as the one used in [2]).

Each converter is controlled using the decoupled dq-control strategy [23]. The rectifier end controls the dc-side voltage (V_{dc}) and the ac-side reactive power (Q_{rect}), while the inverter end controls the ac-side active power (P_{inv}) and reactive power (Q_{inv}). Nearest-level control (NLC) is utilized for submodule switching. A circulating current suppression controller (CCSC) is also included to eliminate the second harmonic component in the MMC's circulating current.

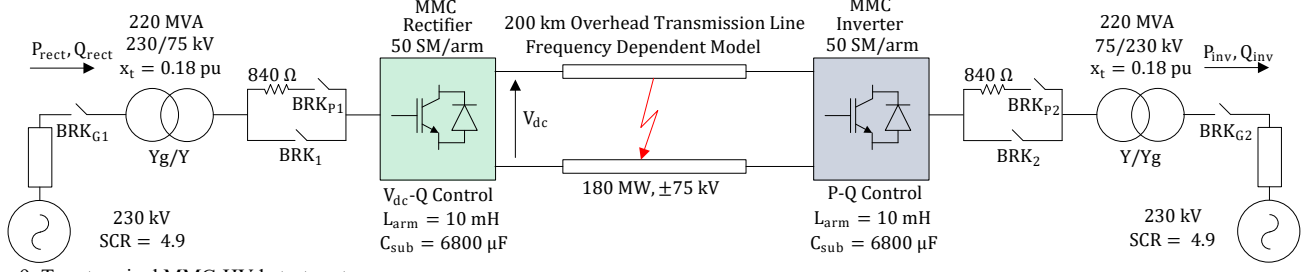For validating the accuracy of the loss estimates obtained

Fig. 9. Two-terminal MMC-HVdc test system

using the proposed approach during steady state as well as transient operation, we consider two scenarios:

(A) Start-up of the MMC-HVdc link.

(B) A pole-to-pole fault at the midpoint of the dc line.

In each of these cases, the loss estimates obtained for the rectifier end MMC using the proposed approach are compared against those obtained from a detailed switching model (DSM) of the rectifier end MMC bridge where each switch is modelled individually. Parameters required for the loss estimation for the ST1500GXH24 IGBT-diode module are given in Table 1. The simulations are carried out in PSCAD/EMTDC with a time-step $\Delta t = 10$ μs.

A. Start-up of the HVdc link

Before starting the HVdc link, both the MMCs are completely blocked (i.e., the gate pulses to all SM switches are 0) and all the ac breakers (viz. BRK_{G1}, BRK_1, BRK_{P1}, BRK_{G2}, BRK_2 and BRK_{P2}) are kept open. In order to gracefully start the link, the following start-up sequence is adopted:

1) At $t = 0.1$ s, BRK_{G1} and BRK_{G2} are closed to energize the converter transformers on both sides.

2) At $t = 0.2$ s, BRK_{P1} and BRK_{P2} are closed to pre-charge the SM capacitors in each of the MMC bridges.

3) At $t = 2.2$ s, BRK_1 on the rectifier side is closed to bypass the BRK_{P1} branch.

4) At $t = 2.7$ s, BRK_2 on the inverter side is closed to bypass the BRK_{P2} branch.

5) At $t = 3$ s, the rectifier end MMC bridge is deblocked to charge the HVdc link to its rated voltage (i.e., ±75 kV).

6) At $t = 3.5$ s, the inverter end MMC bridge is deblocked and the active power (P_{inv}) is linearly ramped-up at the rate of 200 MW/s to the rated value (i.e., 180 MW).

Fig. 10 – Fig. 13 depict the loss estimates (viz. conduction loss, blocking loss, switching loss and total power loss) as a function of time in the rectifier end MMC bridge obtained using the proposed approach. This is compared with the loss estimates obtained using a DSM for the rectifier end MMC bridge in the same plots (Fig. 10 – Fig. 13). Fig. 14 shows the rectifier end active power (P_{rect}) for the two cases.
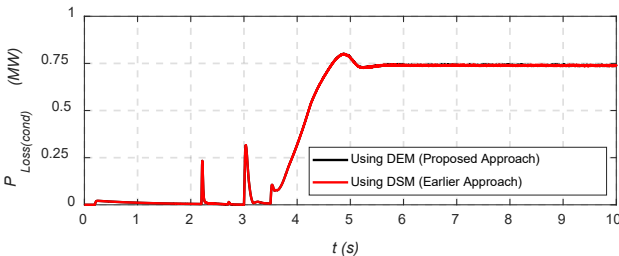
The plots in Fig. 10 – Fig. 13 show that the loss estimates obtained using the two approaches match very closely while starting-up the link as well as in steady state. Thus, this validates the accuracy of the loss estimates obtained using the proposed approach.
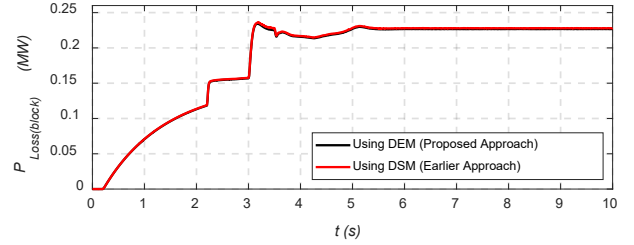

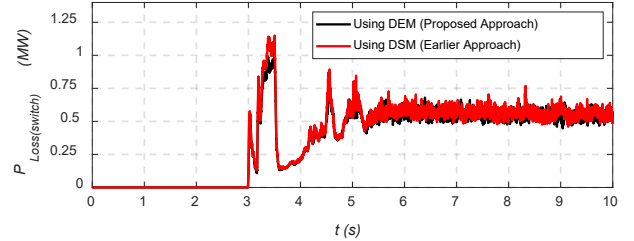Fig. 11. Total blocking loss ($P_{Loss(block)}$) in the rectifier-end MMC bridge

Fig. 12. Total switching loss ($P_{Loss(switch)}$) in the rectifier-end MMC bridge
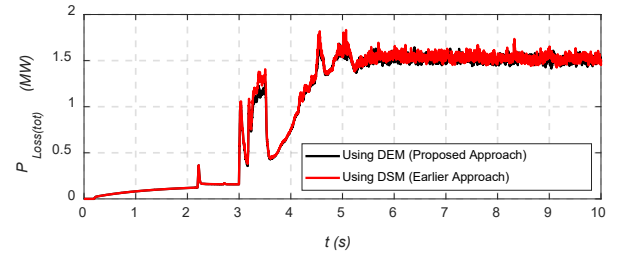

Fig. 13. Total loss ($P_{Loss(tot)} = P_{Loss(cond)} + P_{Loss(block)} + P_{Loss(switch)}$) in the rectifier-end MMC bridge
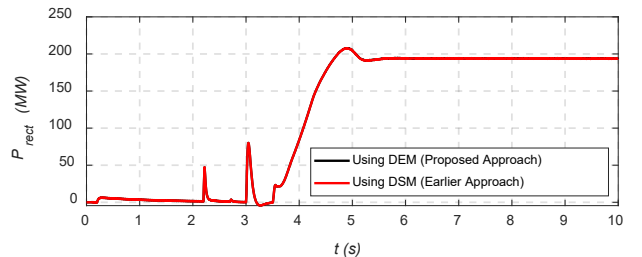

Fig. 14. Rectifier-end active power (P_{rect})

B. Dc side fault

In this case, the HVdc link is initially assumed to be operating in steady state with rated power (i.e., $P_{inv} = 180$ MW) being transferred. At $t = 4$ s, a pole-to-pole dc fault is applied at the mid-point of the transmission line. In order to

Fig. 10. Total conduction loss ($P_{Loss(cond)}$) in the rectifier-end MMC bridge

protect the IGBT switches, the dc fault clearing procedure shown in Fig. 15 is followed [16].
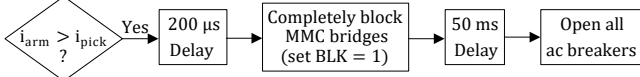

Fig. 15. Dc fault detection and clearing procedure

The pick-up value (i_{pick}) for the MMC arm current (i_{arm}) for the dc fault detection in Fig. 15 is taken to be the rated current (i.e., 1.5 kA) of the ST1500GXH24 IGBT-diode module. In this case as well, the loss estimates (viz. conduction loss, blocking loss, switching loss and total power loss) in the rectifier end MMC bridge obtained using the proposed approach are compared with those obtained using a DSM for the rectifier end MMC bridge. These comparisons are shown in Fig. 16 – Fig. 19. Additionally, Fig. 20 shows the rectifier end active power (P_{rect}) for the two cases.
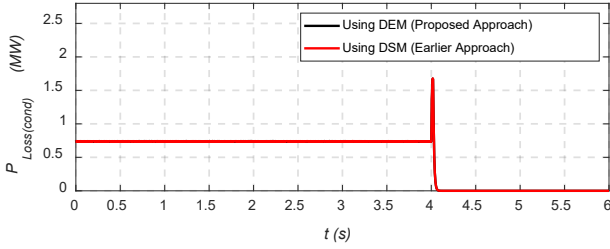

Fig. 16. Total conduction loss ($P_{Loss(cond)}$) in the rectifier-end MMC bridge
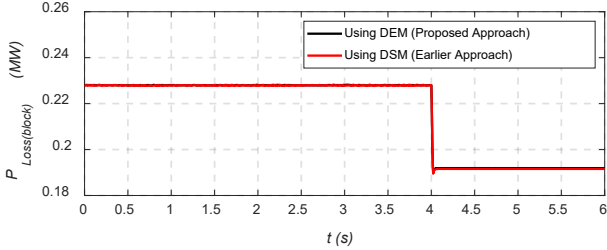

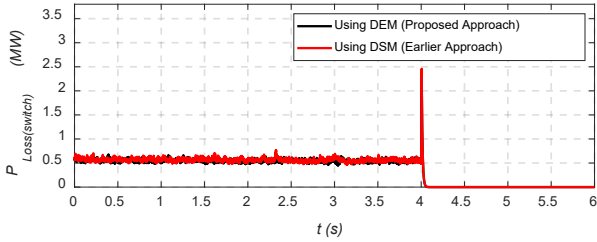Fig. 17. Total blocking loss ($P_{Loss(block)}$) in the rectifier-end MMC bridge

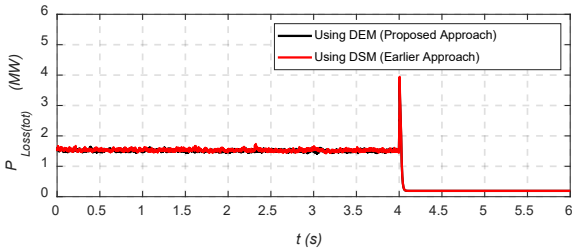Fig. 18. Total switching loss ($P_{Loss(switch)}$) in the rectifier-end MMC bridge

Fig. 19. Total loss ($P_{Loss(tot)} = P_{Loss(cond)} + P_{Loss(block)} + P_{Loss(switch)}$) in the rectifier-end MMC bridge

For this case as well, the loss estimates obtained using the two approaches match very closely not only during steady state but also following a dc side fault, thus validating the accuracy of the proposed approach.
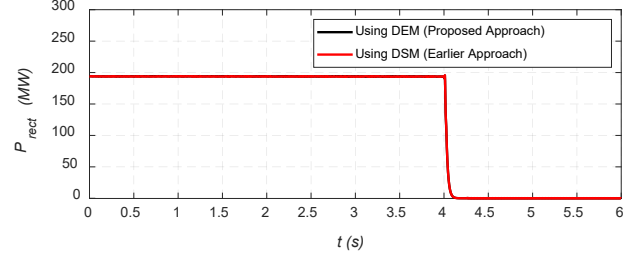

Fig. 20. Rectifier-end active power (P_{rect})

C. CPU Time Comparison

Table 2 gives the CPU time for a simulation which uses the proposed approach and compares it with that for a simulation which uses the earlier approach of estimating the losses at individual switch level (i.e., using DSM). These results are obtained for a 10 s simulation with $\Delta t = 10$ μs. The platform used is a general-purpose Intel i7-8700 based Windows 11 PC having 6 physical cores running at 3.2 GHz.

TABLE 2.
Comparison of CPU Times

Using DEM (Proposed Approach) [T_1]	Using DSM (Earlier Approach) [T_2]	Speedup Factor [T_2/T_1]
196 s (3 min. 16 s)	8646 s (~ 2 hr. 24 min.)	**44.1**

These results show that the proposed approach is able to speed up the loss estimation process by a factor of 44. This clearly demonstrates the superior computational efficiency of the proposed approach for estimating the power semiconductor losses of an MMC as against the earlier approach of estimating them at the individual IGBT-diode component level.

VI. CONCLUSION

In this paper, we present a computationally efficient approach for estimating the power semiconductor losses of an MMC in EMT simulations. The proposed approach coalesces the loss estimation procedure (previously used at individual IGBT-diode component level) with a detailed equivalent model of an MMC arm in order to efficiently estimate the MMC's losses without the need to model each of its switch explicitly. Nevertheless, the proposed approach still allows for reporting the loss estimates of any individual submodule, if required. It is able to estimate the losses during normal operation as well as when the MMC is completely blocked.

A simulation test case of a two-terminal MMC-based HVdc link shows that the proposed approach is able to not only provide accurate and reliable loss estimates, but it also speeds up the loss estimation process significantly as compared to the earlier approach of estimating the losses at individual IGBT-diode component level. Although the approach proposed in this paper is discussed in the context of an MMC using half-bridge SMs, it can easily be extended to other SM topologies as well.

VII. REFERENCES

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