Superimposed Impulse Voltage Test on 525 kV HVDC Underground Cable

I. Radecic, S. Jancin, M. Perkovic, B. Filipovic-Grcic, B. Jurisic, D. Filipovic-Grcic

***Abstract*-- One of the distinctive electrical tests for HVDC cables is the superimposed impulse voltage test. This paper investigates the development and validation of an Electromagnetic Transient (EMT) model for conducting this test on a 525 kV HVDC cable. The model incorporates the actual configuration and parameters of the high voltage (HV) laboratory test circuit. Given the technical challenges posed by the simultaneous application of DC and impulse voltages, the EMT model provides valuable insights into the test circuit's behaviour. Validation with real HV laboratory measurements confirms the model's accuracy and its potential to address these challenges.**

***Keywords*: superimposed impulse voltage test, HVDC cable, HV laboratory testing, EMT simulations**

I. Introduction

The International Energy Agency predicts a 25% increase in overall energy requisites by 2040, with a growing emphasis on the use of HVDC systems in the field of electricity, despite the high costs of converter stations [1]. A critical component of HVDC systems is the transmission medium, either overhead lines or cables, with an increasing number of underground and submarine HVDC cables being installed over ever-greater distances. The choice between overhead lines and cables is primarily determined by environmental impact and overall costs.

HVDC cables are often employed for transmitting large amounts of energy over long distances, where traditional HVAC systems are either not cost-effective or technically unfeasible. The economic design of HVDC cables is increasingly critical, given their substantial contribution to the overall cost of HVDC systems. The feasibility and economic viability of HVDC cable projects can be further enhanced by increasing the power transmission capacity of the cables [1]-[3]. The growing utilization of HVDC cables also necessitates rigorous verification, beginning with type tests to ensure the integrity and continuing with pre-qualification tests to evaluate reliability. Additional requirements include the ability to withstand non-standard dynamic voltage stresses such as polarity reversal and transient overvoltages [2].

A key focus, therefore, lies in managing the thermal load caused by the current flowing through the cable. However, in addition to the enduring stresses at DC operating levels, HVDC cables are also exposed to the risk of transient overvoltage stresses, which pose a significant challenge to the cable insulation system. One of the electrical tests providing insight into the behaviour of cables under such stresses is the superimposed impulse voltage test, described in IEC 62895. The superimposed impulse voltage test is performed after bending test and heat cycle voltage test. It is an integral part of the type test, pre-qualification test, as well as the extended qualification testing procedure. Type tests are conducted prior to the commercial sale of a specific type of cable to demonstrate its satisfactory performance under desired conditions. In contrast, pre-qualification tests aim to confirm the long-term performance of the entire cable system. This is precisely why a cable loop is used as the test object, representing the integrated behaviour of the system.

Overall, type and pre-qualification tests require long-duration procedures. The distinctions between cycles performed under varying polarities and load applications add complexity, making the latter tests more challenging to manage [3]. Moreover, there is a notable difference in the number of cycles required for specific test phases when comparing Line Commutated Converters (LCC) to Voltage Source Converters (VSC) [4]. This distinction arises from the differing operational characteristics and stress factors associated with each converter type, influencing their respective testing protocols.

Additionally, there is also the Extension of the Qualification Test (EQT) test which is conducted to confirm the long-term performance of a cable system that has been previously evaluated. This test is required when substantial changes have been made to the system. A "substantial change" is defined as any modification that could negatively impact the system’s performance [4]. If such changes are introduced, the supplier must provide a detailed case with supporting test evidence, showing that the modifications do not constitute a substantial change to the system’s behaviour or functionality.

The final sequence of all the tests, type, pre-qualification and EQT, is the superimposed impulse test, which serves as a conclusive evaluation to verify the cable system's ability to withstand combined stresses under realistic operating conditions. During superimposed impulse test, the test object shall withstand without failure 10 positive and 10 negative superimposed switching impulses (SI) and 10 positive and 10 negative superimposed lightning impulses (LI) [4]. Conducting this test in the laboratory can be challenging, as different voltages must be applied to the test object

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Paper submitted to the International Conference on Power Systems Transients (IPST2025) in Guadalajara, Mexico, June 8-12, 2025.

simultaneously. Therefore, this test includes additional components in the circuit, which act as a coupling for the generated voltage and as a blocking element for the other type of voltage. Two different test circuits are commonly used for superimposed impulse testing: test circuit with a coupling capacitor or the one with the sphere gap. In [6] and [7] advantages and disadvantages of these test circuits are considered.

Given that this is a complex test requiring numerous components, it is advisable to verify such testing through EMT simulation before its execution in a HV laboratory to check the superimposed impulse voltage parameters (amplitude, front time and tail time). Therefore, the following text describes the test setup in a HV laboratory. It is also presented how each individual real component in the HV laboratory was modelled in the EMTP program. Finally, the simulated waveform of the test voltages is compared with the measured one. The conclusion follows at the end.

II. Test Setup for Superimposed Impulse Test

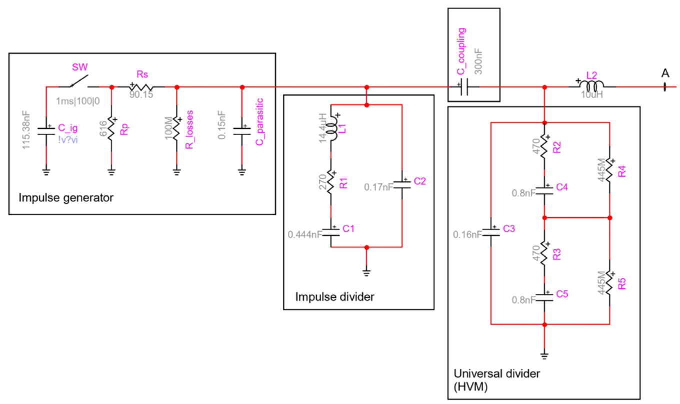
Considering the availability of equipment in the HV laboratory and the advantages of conducting the superimposed impulse voltage test, it was decided to use a test circuit with a coupling capacitor formed from extra or spare upper stages of the impulse voltage generator. The test circuit used in the HV laboratory is shown in Fig. 1.

Fig. 1. Test setup in HV laboratory for superimposed impulse test (1 – impulse generator; 2 – test object (here a capacitor, but in observed case the DC cable test loop was used); 3 – impulse divider; 4 – universal divider; 5 – DC voltage generator)

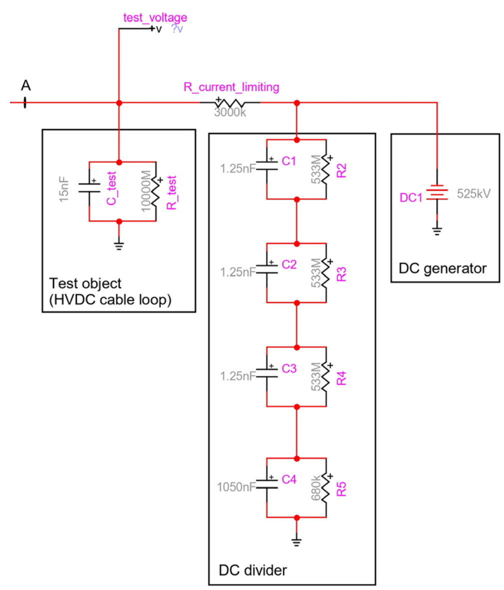
There must be two voltage sources, a DC source and an impulse voltage generator. Additionally, control measurements are required, such as the impulse divider, which is used to verify the characteristics of the impulse voltage. The voltage on the test object is measured using a universal divider, which is ultimately the only parameter crucial for the evaluation of the test.

The DC voltage generator is protected by a current-limiting resistor, which must be properly dimensioned to safeguard the DC side from superimposed impulse voltage. Additionally, the impulse generator needs protection from the DC voltage. The coupling capacitor-based test circuit involves permanently connecting the impulse generator to the test object through a coupling capacitor. This capacitor acts as an open circuit (high impedance) for DC voltage, effectively protecting the impulse generator from it. From the perspective of the impulse generator, the coupling capacitor behaves as a short circuit (low impedance) for fast front impulse voltages containing high frequencies. This allows the impulse voltage to be efficiently injected into the test object through the coupling capacitor.

Once the method and test setup have been defined, an EMT simulation of the test circuit can be performed, where each HV component is modelled individually. Thus, based on Fig. 1., an EMT model of the test circuit was created. The resulting EMT model is shown in Fig. 2., which is divided into two segments for improved clarity and better visualization.



a) EMTP model – segment 1/2



b) EMTP model – segment 2/2

Fig. 2. EMT model of the HV laboratory test setup for superimposed impulse voltage test

The test object, in this case a cable loop, is represented as a parallel equivalent capacitance and resistance. While lumped capacitance and resistance simplifies the analysis, HVDC cables are typically modelled using a more detailed distributed and frequency dependent parameter model when the cable's length is comparable to the wavelength of the impulses being applied. In this case, total length of the test loop is approximately 80 meters, which is relatively short compared to the wavelength of typical lightning impulse signals, so a lumped model still provides a reasonable approximation, particularly for the voltage response during the impulse test. During such tests, the cable's capacitance to ground plays a crucial role in how quickly the voltage distributes along the cable during the fast front of the impulse. For a lumped capacitance model with resistance to be valid in this case, the key assumption is that the signal's rise time is fast enough that the propagation delay across the loop is negligible relative to the overall response time. When considering the cable loop as a closed circuit and focusing on how the cable charges due to the lightning impulse, the entire system can be simplified by modelling the cable's total capacitance to ground as a single lumped element. The distributed nature of the capacitance becomes less relevant since the impulse is applied at a single point, and the loop's behaviour can be approximated as if the capacitance is concentrated at the point where the impulse is injected. For practical reasons, it is also reasonable to use a simple model of a test object to have a possibility of fast estimation for the generated waveshapes.

What changes in EMT model, depending on whether it is an LI or SI test, are the parameters of the impulse generator model and its initial charging voltage. The impulse generator is characterized by a series resistor R_s, a parallel resistor R_p, and an equivalent capacitance C_{ig}, as well as parasitic capacitance and resistance. In the case of a SI, the values are R_s = 3861.5 Ω, and R_p = 31500 Ω, while for a LI, they are R_s = 90.15 Ω and R_p = 616 Ω. These resistor values are used to adjust the front time and time to half of the output voltage waveform. The equivalent capacitance C_{ig} is 115.38 nF and remains constant regardless of whether it is an SI or LI, as it determines the energy of the impulse. Otherwise, the test circuit is the same.

After the EMT model and the HV test configuration are established, the created EMT model can be validated with real measurements. Therefore, in the following section, a comparison is made between the results obtained from the simulation and the actual measurements on the real test object.

III. Superimposed Impulse Voltage Test Verification of the EMT Model

The superimposed impulse voltage test involves a total of six different voltage waveforms with various polarities, in accordance with [4] and [5]. The SI is applied to both positive and negative DC voltages, meaning it is used with both matching and opposing polarities relative to the DC source. On the other hand, the LI is applied only to the opposite polarity of the DC source. Simply put, a positive SI will be applied to both a positive and a negative DC source, and the same applies to a negative SI. However, a positive LI will only be applied to a negative DC source, while a negative LI will be applied to a positive DC source. Although there are six different waveforms, the test configuration remains the same, with only the polarity of the sources being reversed or the impulse generator settings adjusted according to the desired impulse.

A 525 kV underground HVDC cable was brought to the HV laboratory for EQT. The EQT testing consists of several sequences, which differ between LCC and VSC, as is shown in Table 1. These sequences include load cycle (LC), power reversal (PR), high load (HL), zero load (ZL), and superimposed impulse voltage (S/IMP). This paper focused on the S/IMP sequence of testing, where the actual test object was evaluated in the HV laboratory.

TABLE I
EQT Sequences for LCC/VSC Systems [4]

LCC Systems										
	LC	LC	LC + PR	HL	HL	ZL	LC	LC	LC + PR	S/IMP
Number of cycles or days	4 cycles	4 cycles	12 cycles	18 days	18 days	6 days	4 cycles	4 cycles	12 cycles	N/A
Test Voltage	+	-		+	-	-	+	-		$U_{P2,0}$=1.2U_0 U_{P1}=2.1U_0
	U_{EQ1}	U_{EQ1}	U_{EQ2}	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ2}	

VSC Systems								
	LC	LC	HL	HL	ZL	LC	LC	S/IMP
Number of cycles or days	10 cycles	10 cycles	18 days	18 days	6 days	10 cycles	10 cycles	N/A
Test Voltage	+	-	+	-	-	+	-	$U_{P2,0}$=1.2U_0 U_{P1}=2.1U_0
	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ1}	U_{EQ1}	

* U_0 is the rated continuous DC voltage between conductor and core/insulation screen for which the cable system is designed; U_{EQ1} and U_{EQ2} are DC voltages during the EQT (U_{EQ1}=1.68U_0 and U_{EQ1}=1.37U_0); $U_{P2,0}$ is 1.15 × the maximum absolute peak value of the SI voltage which the cable system can experience when the impulse has the opposite polarity to the actual DC voltage; U_{P1} is 1.15 × the maximum absolute peak value of the LI voltage which the cable system can experience when the impulse has the opposite polarity to the actual DC voltage

An EMT model based on the test circuit was then created and subsequently validated through measurements. This approach ensured the model's accuracy and its capability to replicate the test conditions effectively.
The test sample, a copper conductor with XLPE insulation, was analysed in the HV laboratory using the test setup shown in Fig. 1. To replicate real-life conditions as accurately as possible, the test sample includes two joints and one termination, ensuring all components are qualified. It is common practice to test a test loop comprising multiple elements, rather than just a single cable [4]. The total length of the test loop is approximately 80 meters.

Once the test object is set up, the testing begins according to IEC 62895. The first step is the bending test, followed by a visual inspection to ensure no damage has occurred to the test sample. This is followed by the heat-cycle voltage test, along with other specifications per the client's requirements. However, the focus of this article is the superimposed LI and SI voltage test, the details of which are explained in CIGRÉ TB 852 [4]. During the application of all superimposed voltage waveforms, insulation breakdown did not occur at the test object.

Afterwards, EMT simulations were performed and compared with the measurement results. Fig. 3. – 8. illustrate the comparison of voltage waveforms applied to the test object. The EMT simulation was conducted using the model shown in Fig. 2. The test object is represented as a parallel circuit consisting of a substitute capacitance of 15 nF and a high resistance. This approach enables the execution of an EMT simulation, which can then be used to validate the results obtained from the HV laboratory tests.

Analysing Fig. 3. – 8. reveals that the waveforms obtained from measurements closely align with those from EMT simulations, validating the EMT model of the test circuit. This validated EMT model can be employed for future tests to assess their feasibility and parameter optimization. Verification and understanding of the superimposed impulse test are significant, as it is an integral part of HVDC cable testing. An important technical aspect of this test is coupling capacitor connection.

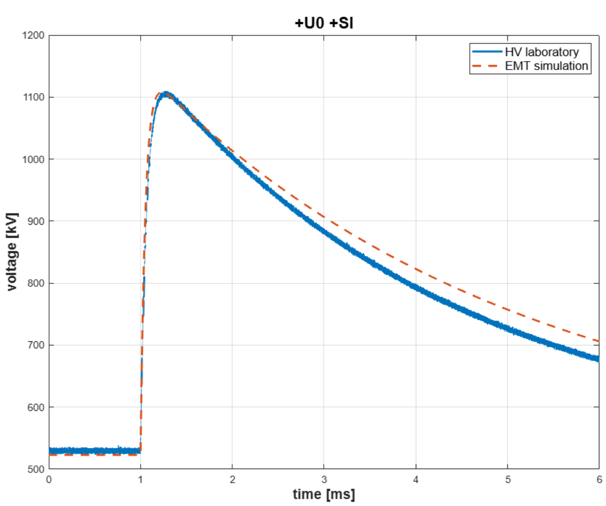


Fig. 3. Same polarity, positive SI – comparison of EMT simulation and HV measurement

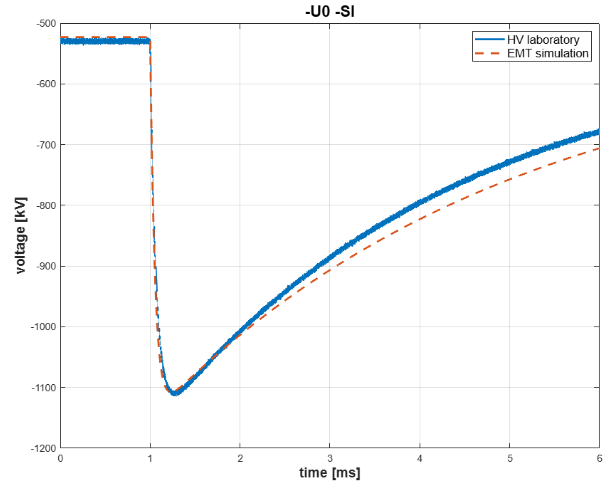


Fig. 4. Same polarity, negative SI – comparison of EMT simulation and HV measurement

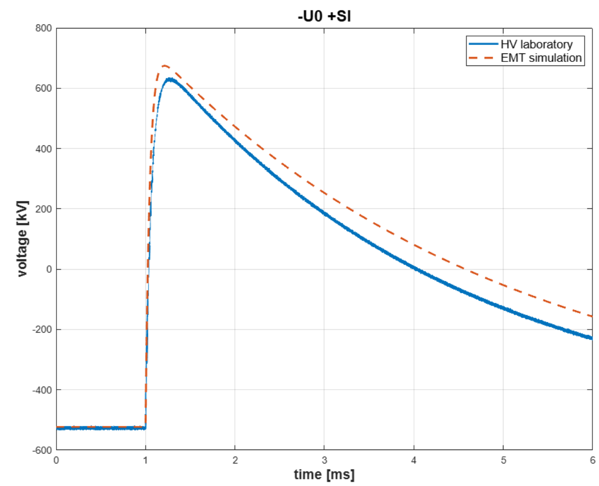


Fig. 5. Opposite polarity, positive SI – comparison of EMT simulation and HV measurement

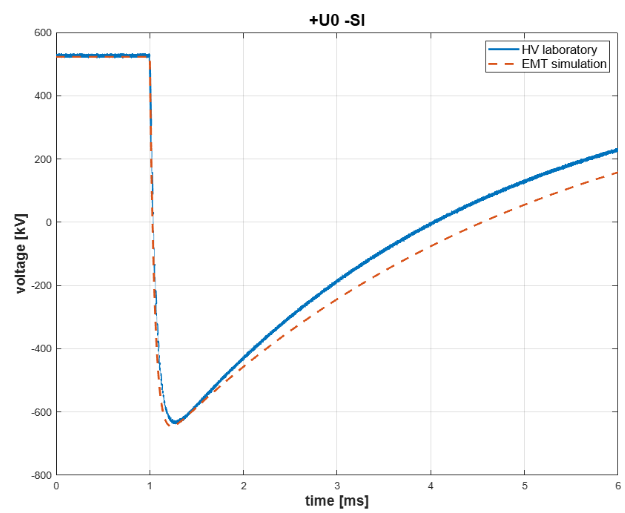


Fig. 6. Opposite polarity, negative SI – comparison of EMT simulation and HV measurement

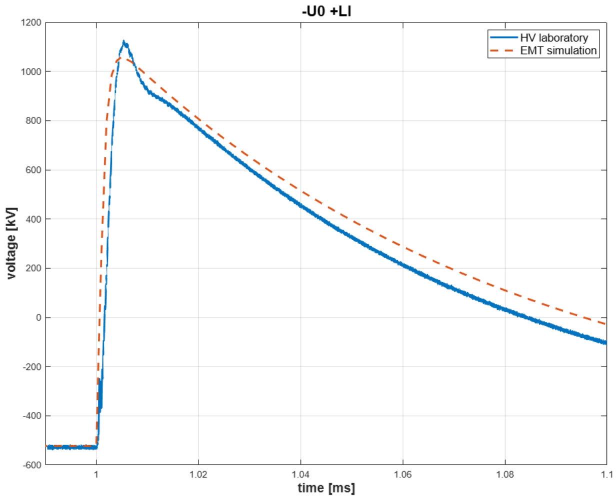


Fig. 7. Opposite polarity, positive LI – comparison of EMT simulation and HV measurement

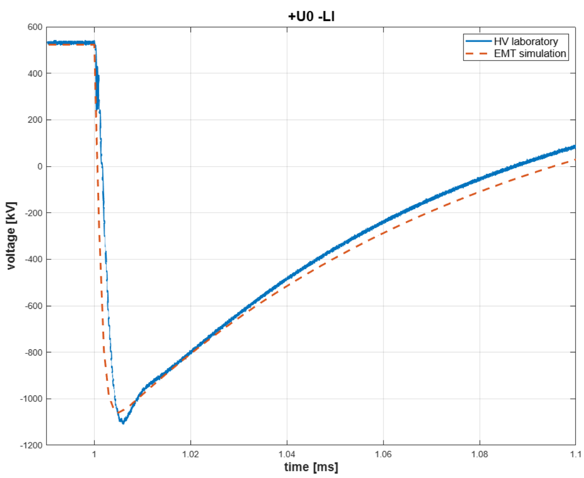


Fig. 8. Opposite polarity, negative LI – comparison of EMT simulation and HV measurement

IV. Coupling Capacitor Connection

The coupling capacitor is commonly implemented using the uppermost stages of the impulse voltage generator, as they are suitable in terms of capacitance and voltage rating. However, this requires a specific connection method to address voltage redistribution, which can be a critical parameter for the impulse voltage generator [8].

A practical solution to realize coupling capacitor is to use extra or spare upper stages of the impulse voltage generator. Charging capacitors of the impulse generator have appropriate capacitance and voltage rating making them an attractive solution for DC coupling capacitor. There are two common types of impulse generators with respect to charging, unipolar and symmetric, which have different connection schemes per stage and between stages. If upper stages' capacitors of impulse generator with unipolar charging are used as coupling capacitor, sufficient number of these needs to be connected in series and the easiest way to link them is to replace series resistors with conductive link bars. This easy action will give ideal voltage distribution (Fig. 9 left).

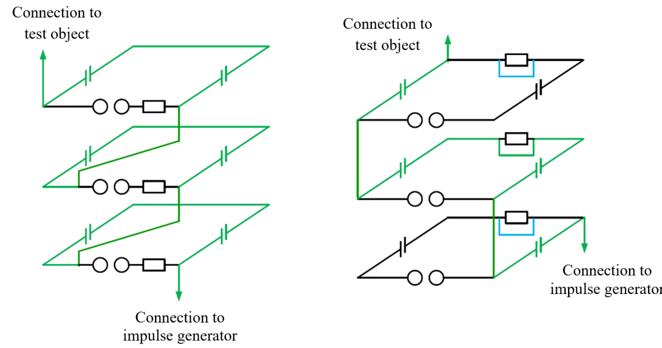


Fig. 9. Coupling capacitor formed from upper stages of unipolar charging generator (left) and symmetrical charging generator (right)

Impulse generators with symmetrical charging are not that user friendly when coupling capacitor needs to be formed. Simple action of replacing the series resistors by link bars alone is not appropriate since only one capacitor per stage shall be utilized. Therefore, another connection scheme is commonly used as shown in Fig. 9 (right), which has two drawbacks: first, one capacitor on the lowest coupling capacitor stage and one capacitor on the upper most stage cannot be utilized and second, voltage distribution is far from ideal resulting in double voltage stress per stage as compared to unipolar charging generators. Two unused capacitors means that an extra impulse generator stage must be available which increases height of the generator and reduces the clearance to HV laboratory ceiling.

To overcome these disadvantages, alternative connection is proposed in which jumpers are placed over sphere gaps (Fig. 10) and series resistors are replaced with link bars.

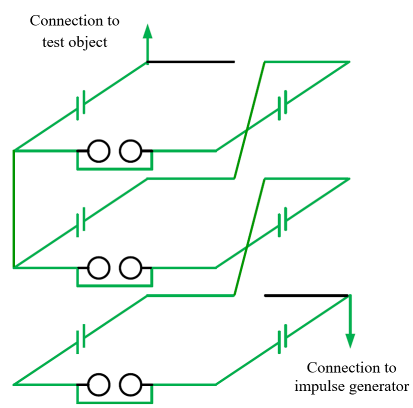


Fig. 10. Coupling capacitor formed from the upper stages of a symmetrical charging generator, alternative connection

Benefits of this connection are that voltage distribution is ideal, and all capacitors are used, but special attention must be paid to jumper design, positioning and dimensioning.

V. Conclusion

The superimposed impulse voltage test is an integral part of the type test, pre-qualification test, and the extension of qualification test for HVDC cables. The practical execution of the test is complex, as both DC voltage and impulse voltage must be applied simultaneously. Adequate coupling and blocking elements are inserted between the test object and test equipment to ensure proper operation. To connect an impulse generator, two commonly used options are the coupling capacitor and the sphere gap.

This paper presents the validation of an EMT model, developed based on testing of a 525 kV underground HVDC cable in the HV laboratory. The method used in this paper employed a coupling capacitor for the configuration. The challenge lies in forming the coupling capacitor from the uppermost stages of the impulse generator and determining how to connect them to achieve a linear voltage distribution. Alternative connection is proposed which was used successfully during the superimposed impulse voltage test on HVDC cable in HV laboratory.

EMT simulations are successfully used to accurately assess the test circuit conditions and to check the expected superimposed impulse voltage parameters (amplitude, front time and tail time) prior to testing, and to verify the generator connection method.

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