Application of Fault Current Bypassing Method Using Double-Thyristor Module on Full-Bridge MMC based AC/DC Hybrid Distribution System

Ho-Young. Kim, Gwang-Su. Shin, Jin-Sol Song, Chul-Hwan Kim

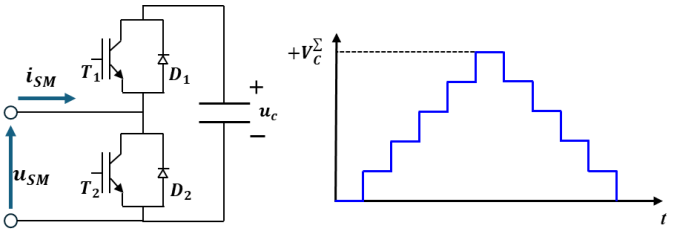
***Abstract*— With the growing interest in reducing carbon emissions, the integration of Renewable Energy Source(RES) is becoming more active. Recent studies have shown that constructing an AC/DC hybrid power system, rather than connecting individual power conversion devices to the traditional AC power system, is more effective in reducing power conversion losses. This AC/DC hybrid power system is based on the Modular Multilevel Converter(MMC), which can be categorized into Half-Bridge MMC(HB-MMC) and Full-Bridge MMC(FB-MMC) depending on the type of submodules. In this paper, we verified the effectiveness of applying a bypassing method using thyristors to a FB-MMC equipped with a blocking function when Pole-to-Pole(PTP) fault occurs by comparing the di/dt using Matlab/Simulink software.**

***Keywords*: AC/DC Hybrid Distribution system, Double Thyristor Module, Fault current bypassing method, FB-MMC**

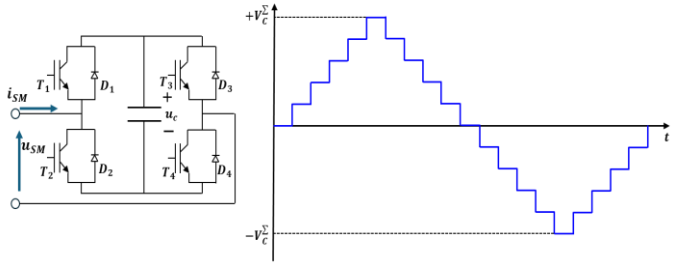
I. Introduction

To achieve carbon emission reduction targets and carbon neutrality, countries around the world have proposed various policies aimed at increasing the integration of renewable energy and developing Direct Current (DC) distribution systems. In particular, '10th Basic Plan for Electricity Supply and Demand' of the Republic of Korea predicts an increase in DC power demand due to the expansion of electric vehicles and the growing number of data centers[1]. Additionally, 'the 4th Energy Technology Development Plan' sets the development of DC transmission and distribution systems as a goal to accommodate the increasing amount of RES integration[2]. There has been a growing interest in AC/DC hybrid distribution networks, which utilize both AC and DC distribution systems. AC/DC hybrid distribution networks offer the advantage of reducing power conversion losses compared to installing individual power conversion devices when integrating DC-based RES or loads into the existing AC distribution grid, and related research is actively being conducted.

The AC/DC hybrid distribution network is based on MMC and can be classified into HB-MMC and FB-MMC depending on the type of submodules used. Fig. 1 illustrates the basic topology of each MMC and the voltage levels that can be output when utilizing strings composed of the respective submodules, where (a) corresponds to HB-MMC and (b) corresponds to FB-MMC. In MMC-based AC/DC hybrid distribution system, unlike conventional AC distribution networks, research is needed on protection strategies within the MMC to limit fault currents in preparation for DC-side faults. One such strategy involves modifying the topology of the MMC. [4] proposed a method that combines HB-MMC modules with thyristor-based MMC modules, while [5] suggested a method that combines FB-MMC modules with HB-MMC modules. Another approach is the fault current bypassing method. In [6], single thyristor modules and double thyristor modules were used, and fault currents was calculated when applying the bypassing method. Additionally, it was verified that the performance of the double thyristor module was superior. However, most research focus on HVDC systems based on MMC or employ HB-MMC, thereby overlooking the blocking sequence of FB-MMC. In this paper, we applied double thyristor modules to FB-MMC, including the blocking sequence of the Insulated Gate Bipolar Transistor (IGBT), and compare the *di/dt* stress on the MMC to verify the effectiveness of the bypassing method during PTP fault. The rest of this paper has been structured as follows. Section II contains explanations about characteristics of DC fault and principle of current bypassing method using thyristor modules. Section III presents simulation conditions and results of current bypassing method in FB-MMC based MVDC test system. Finally, section IV and V contains discussions and conclusions of this paper.



(a) HB-MMC



(b) FB-MMC

Fig. 1. Topology of each MMC and the possible output voltage levels. (a) HB-MMC, (b) FB-MMC [3]

II. Fault Current Bypassing Method

In this section, fault current bypassing method using double thyristor module is introduced which artificially create three phase AC short circuit so that fault current contributed from AC side can be offset.

A. Stage of PTP fault current[7]

PTP faults can be divided into three stages. In stage 1, each submodule is not blocked, and the fault current increases rapidly due to the discharging of the capacitors, while the fault current contributed by the AC side also flows to the DC side. In stage 2, the reactors in each arm discharge continuously, and since the three-phase fault current contributed by the AC side flows to the DC side, overcurrent occurs. In stage 3, the operation is similar to that of a rectifier, and due to the low impedance, a larger fault current persists compared to AC faults. However, in FB-MMC based MVDC system, due to blocking sequence of FB-MMC, fault current will be blocked in the early stage of PTP fault. The example of fault current blocking sequence based on MMC arm current is shown in Fig. 2.

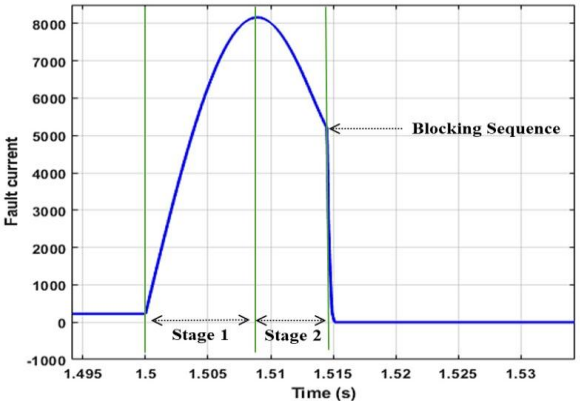


Fig. 2. Example of fault current with FB-MMC blocking sequence

B. Principle of current bypassing method[6]

Fig. 3 shows the fault current path to explain the principle of applying the fault current bypassing method to an FB-MMC. During a PTP fault, a three-phase short circuit is formed as shown in fig. 3 by switching on the thyristors connected to each submodule. This offsets the fault current component contributed by the AC side, preventing it from flowing to the DC side. In the case of the thyristor module, the thyristor remains in an off-state during normal operation, but when a PTP fault occurs, it switches to the on-state, allowing the fault current to flow through the thyristor, leading the DC fault current to decay to zero.

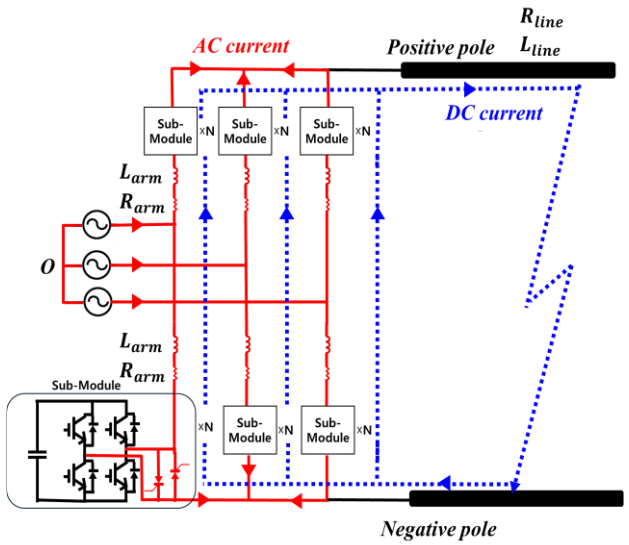


Fig. 3. Fault current path during PTP fault

The fault current calculation formula can be derived using the circuits seen from each pole to the AC side and the PTP fault side. By applying Kirchhoff's Voltage Law (KVL) to the three phases of the upper arm and lower arm and utilizing the fact that the current of the DC link has the opposite sign to the sum of the three-phase currents, the voltage equation of the DC link can be derived. Additionally, by comparing the DC link voltage equation obtained from the KVL of the circuit seen from each pole to the PTP fault side and expressing it in the form of a first-order differential equation, the solution can be obtained to calculate the DC fault current as shown in Equation (1)[6].

$$i_{dc}(t) = I_0 e^{-(t-t_0/\tau)} \tag{1}$$

where

t_0: time when all thyristors are switched on

I_0: current value when all thyristors are switched on

τ: time constant$\left(= \left[L_{line} + \left(\frac{2}{3}\right) L_{arm}\right] / [R_{line} + \left(\frac{2}{3}\right) R_{arm}]\right)$

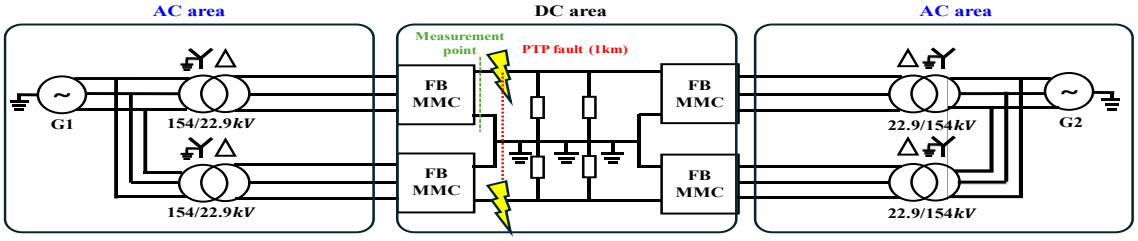


Fig. 4. Test system diagram

III. SIMAULATION CONDITIONS AND RESULTS

A. Simulation conditions

In this paper, the fault current bypassing method was applied in an AC/DC hybrid distribution system based on a FB-MMC configured in a symmetric bi-polar structure, assuming a Point-to-Point configuration. The parameters for the lines/cables were modeled based on the ACSR-160 line data, with a resistance of 0.0182 [ohm/km]. The total line length between the MMCs is 5 km, and a double thyristor switch module is installed in each MMC. The number of submodule for each arm is 16 and double-thyristor module is connected parallel to each sub module. The test system diagram is shown in Fig. 4. The blocking sequence and bypassing method are modeled to operate based on overcurrent measured in each arm. Prior to a fault, each submodule operates normally. However, when a PTP fault occurs, if the overcurrent in the upper and lower arms exceeds the threshold value of 1.8 [p.u.] (rms), a blocking signal is sent to each IGBT, or a thyristor module is activated to provide a bypassing path. Table I presents the detailed parameters of the simulation system and the MMC.

TABLE I. TEST SYSTEM PARAMETER

Category		Value
Network	Rated voltage (DC)	±**20** [kV]
	Length of cable	5 [km]
	Location of fault	1 [km]
	Fault time	1.5 [s]
MMC	Arm inductance	0.1438 [p.u.]
	Arm resistance	0.0014 [p.u.]
	SM capacitance	4 [mF]
	Number of submodules per arm	16
	Threshold current for block(arm current, rms)	1.8 [p.u.]
	On-state resistance (thyristor)	0.00875 [ohm]
	On-state inductance (thyristor)	0.003 [ohm]

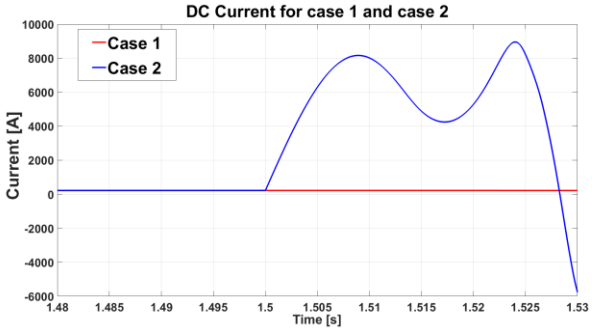
Furthermore, five cases were classified to verify the effectiveness of the double thyristor module. Case 1 represents the base case where PTP fault does not occur. Cases 2 ~ 5 involve scenarios where a PTP fault occurs at the 1 [km] point after 1.5 [s]. Case 2 is also base case and assumed that the IGBT blocking sequence does not operate, and the bypassing method is also not applied. This condition is set for comparison with case 3 ~ 5. Case 3 is assumed that the bypassing method is not applied, but the IGBT blocking sequence is operational, based on the arm current threshold value of 1.8 [p.u.]. In case 4, in contrast to case 3, the bypassing method is applied, but the blocking sequence does not operate, and the switch of the bypassing module is assumed to turn on after 3 [ms]. Finally, case 5 is assumed where the bypassing method is applied, and the blocking sequence is successfully executed. This is summarized in table II.

TABLE II. CONDITION OF EACH CASE

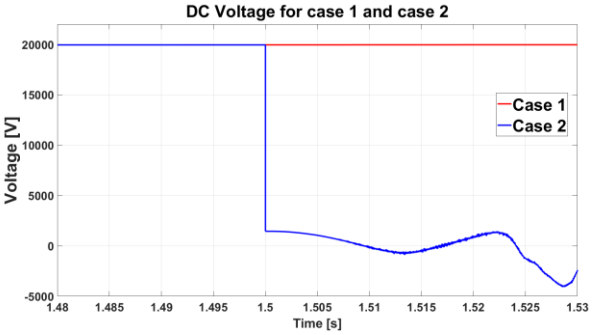
Case number	Fault	Blocking	Bypassing
1	X	X	X
2	O	X	X
3	O	O	X
4	O	X	O
5	O	O	O

B. Simulation results

Since DC-side faults must be cleared rapidly within 5 to 20 [ms], waveforms for all cases were observed up to approximately 30 [ms] after the fault occurrence. The current and voltage waveforms for case 1 and case 2, which are used as a base case for comparison, are shown in Fig. 5. In case 1, since no fault occurred, the current and voltage values remain constant as 220[A] and 20 [kV]. In case 2, due to the PTP fault, the voltage decreases and the current rises rapidly. At this time, the first peak current reaches 8.1 [kA] at 1.508 [s].



(a) DC current

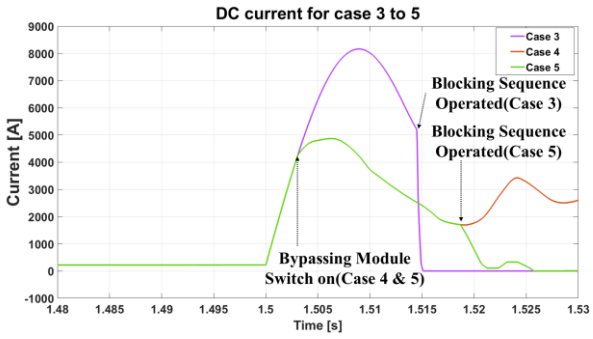


(b) DC voltage

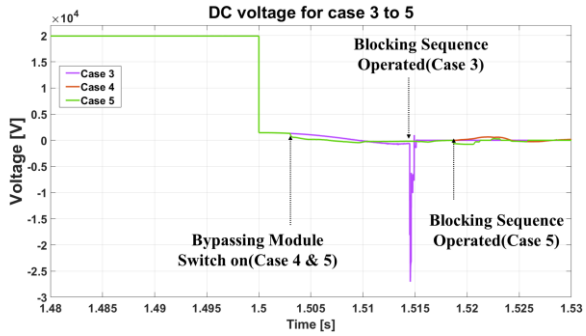
Fig. 5. DC current and voltage for case 1 and case 2

Fig. 6 shows the current and voltage waveforms for case 3 to 5. In case 3, due to the operation of the blocking sequence, approximately 14.5 [ms] after the fault occurred, the current was blocked, and at this point, the voltage exhibited a significant negative peak. In cases where the fault current bypassing method was applied, such as in case 4 and case 5, the thyristor switched on 3 [ms] after the fault occurred, reducing the fault current peak to approximately 4.8 [kA]. Additionally, in case 5, the blocking sequence activated 18.7

[ms] after the PTP fault, resulting in the current being interrupted, as shown in the current waveform. The voltage waveform exhibited similar differences between the cases, with changes observed at 3 [ms] and 18.7 [ms].



(a) DC current



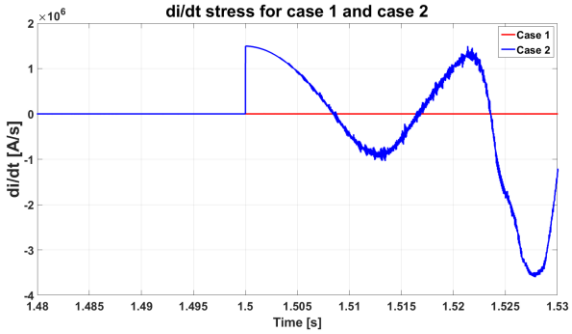
(b) DC voltage

Fig. 6. DC current and voltage for case 3 ~ 5

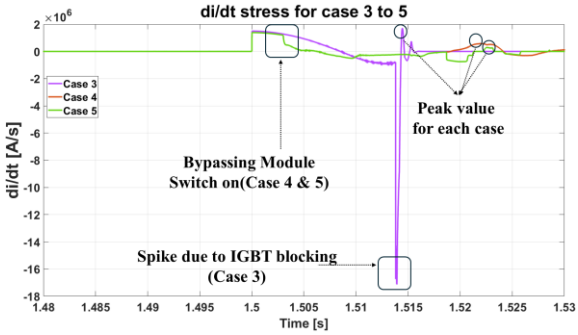
The di/dt stress for the base cases, case 1 and case 2, are shown in Fig. 7 (a). In case 1, where no PTP fault occurs, the di/dt stress value remains close to zero. In contrast, in case 2, it can be observed that di/dt increases significantly right after the fault occurs, with a peak value of 1,495,000 [A/s]. Furthermore, approximately 21 [ms] after the fault occurs, a large value of around 1,300,000 [A/s] is observed. Fig. 7 (b) presents the di/dt stress for case 3 to 5. In case 3, the di/dt value shows a high peak of 1,495,000 [A/s] right after the fault occurs and 1,682,000 [A/s] immediately after the blocking operation. This confirms that not only does the fault immediately after its occurrence cause significant di/dt stress on the MMC, but the operation of the blocking sequence also contributes to substantial di/dt stress. In case 4 and 5, di/dt values are identical up to approximately 18.7 [ms] after the fault occurs, but differences emerge after the blocking sequence is triggered. Due to the bypassing of the thyristor module, a smaller di/dt value is observed starting from 3 [ms] after the fault occurrence compared to case 3, and the subsequent peak value is also reduced compared to Case 3. Additionally, case 5 shows a lower di/dt value than case 4. In case 4, the di/dt value reached 599,600 [A/s] at 21.8 [ms] after the fault occurrence, while in case 5, it reached 277,500 [A/s] at 22.5 [ms] after the fault occurrence. Fig. 7 (c) presents blocking signal of IGBT in case 3 and case 5. This indicates that the blocking operation is slightly delayed due to the bypassing method. Also, Table III shows summarization of simulation results except base cases. Also, summarization of result that fault location is varied to 0, 1, 2 [km] in Table IV.

TABLE III. SUMMARIZATION OF CASE 3 TO 5

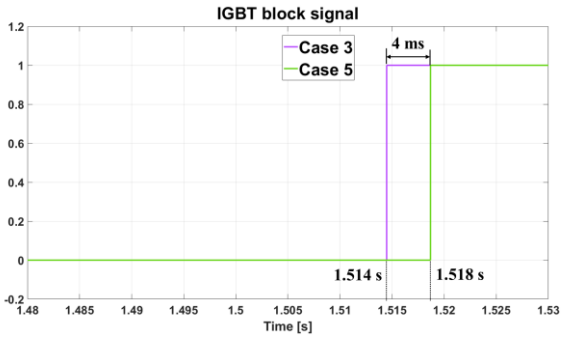
Case number	Peak value of current [kA]	Peak value of *di/dt* [A/s]	Reduction rate of *di/dt* value [%]
3	8.1	1,682,000	-
4	4.8	599,600	64.4
5	4.8	277,500	83.5



(a) case 1 and 2



(b) case 3 ~ 5



(c) Blocking signal in case 3 and case 5

Fig. 7. di/dt stress for each case and blocking signal in Case 3 & 5

TABLE IV. SUMMARIZATION OF RESULT FOR VARIABLE FAULT LOCATION

Case number		Peak value of current [kA]	Peak value of *di/dt* [A/s]
3	0 [km]	8.1	1,469,000
	1 [km]	8.1	1,682,000
	2 [km]	8.2	1,744,000
4	0 [km]	5.9	1,465,000
	1 [km]	4.8	599,600
	2 [km]	7.7	1,347,000
5	0 [km]	4.7	1,700,820
	1 [km]	4.8	277,500
	2 [km]	4.7	1,787,000

IV. Discussions

Through the comparison of case 1 and case 2, a significantly large fault current is observed during a PTP fault occurrence, and case 3 confirms the interruption of the fault current via the IGBT's blocking sequence within the FB-MMC. However, it is evident that when only the blocking sequence is active, the di/dt stress applied to the MMC immediately afterward is very high and critical. This indicates that relying solely on the IGBT blocking in the FB-MMC has limitations for the stable operation of the AC/DC hybrid distribution system. To mitigate this issue, this paper applied a double thyristor module, and the effectiveness of this approach is validated through the results of case 4 and case 5. By comparing the results of case 3 with case 4 and 5, it is confirmed that the application of the bypassing method can reduce the di/dt stress on the MMC. Notably, the results from case 5 demonstrate that when the IGBT blocking and bypassing methods are implemented in parallel, the blocking operation based on a threshold determined by the rms value of the arm current can still be activated, resulting in a reduction in the di/dt stress applied after the blocking operation. Analyzing the results based on the fault locations in Table 4, it was observed that when the bypassing method was applied, the peak value of the fault current and the di/dt value were smaller compared to when only the blocking sequence was used. In this paper, since different operational times for IGBT blocking and thyristor switch-on are assumed, it is considered necessary to conduct a comparison with cases where the operational times of both methods are aligned. Additionally, it is seemed essential to determine the optimal operational timing for these methods. Also, in case of double-thyristor module and FB-MMC, they have lot more components than conventional HB-MMC based AC/DC hybrid system. It could be disadvantageous from a cost perspective.

V. CONCLUSION

In this paper, a double thyristor module was applied to a test system for an AC/DC hybrid distribution system based on an FB-MMC configured in a symmetric bi-polar structure, assuming a Point-to-Point configuration. The effectiveness of the fault current bypassing method was demonstrated by comparing the di/dt stress on the MMC. Through five cases, the impact of applying IGBT blocking and the bypassing method was examined, and the results of case 3 to 5 showed a reduction of approximately 64.4[%] and 83.5[%] in di/dt stress. Future research will focus on developing MMC fault current limiting techniques by optimizing the operation times between the two methods.

VI. ACKNOWLEDGMENT

This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry & Energy (MOTIE) of the Republic of Korea (No.20225500000110).

VII. References

[1] Ministry of Trade, Industry and Energy, “10th Basic Plan for Electricity Supply and Demand”, 2023.

[2] Ministry of Trade, Industry and Energy, “the 4th Energy Technology Development Plan”, 2019.

[3] Kamran Sharifabadi, Lennart Harnefors, Hans-Peter Nee, Staffan Norrga, and Remus Teodorescu, “Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems,” John Wiley & Sons, 2016, pp. 24–25.

[4] B. Bertil, N. Staffan, and J. U. Tomas, “Fault current limitation in DC power transmission systems,” Patent WO 2011029480, Sep. 11, 2009.

[5] J. Hu, K. Xu, L. Lin, and R. Zeng, “Analysis and enhanced control of hybrid-MMC-based HVDC systems during asymmetrical DC voltage faults,” IEEE Transactions on Power Delivery, vol.32, no.3, pp. 1394–1403, Jun. 2017.

[6] Xiaoqian Li, Qiang Song, Wenhua Liu, Hong Rao, Shukai Xu, and Licheng Li, “Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems”, IEEE Transactions on Power Delivery, vol.28, no.1, pp. 483-490, Jan, 2013

[7] Zainan Li, Ke Jia, Tianshu Bi and Juntao Li, “ACLC Control in Half-Bridge MMC for DC Fault”, IEE Transactions on Industrial Electronics, 2024.