Comparative Analysis of Losses in Converters for Battery Energy Storage Using EMT Simulations

Dilsha Kuranage, Shaahin Filizadeh, Ioni Fernando

***Abstract*—The paper presents a comprehensive analysis of losses in several battery energy storage system (BESS) converters using EMT simulations. The work is motivated by the critical need to determine converters' semiconductor losses, particularly due to the high-frequency dc-dc converters that interface batteries. Two general classes, namely modular multilevel and two-level converter topologies, are considered. A simulation-based, computationally efficient, and accurate loss calculation method, which utilizes device data sheet loss curves, is used to estimate semiconductor losses based upon post-processing of EMT simulation results of the converters. The paper quantifies the impact of switching frequency and circulating current suppression controller on the losses. Comparative assessments of the merits of each topology are also presented.**

***Keywords*—Electromagnetic transient (EMT) simulations, modular multilevel converters (MMC), semiconductor losses, battery energy storage.**

I. Introduction

INCREASING penetration of renewable generation resources has reduced the inertia of modern power systems, causing significant power quality and reliability issues [1], [2]. These problems can be largely mitigated by integrating energy storage (ES) to the grid, as it can provide voltage and frequency support by judiciously releasing or absorbing energy [1], [2].

Among various types of energy storage, battery energy storage systems (BESSs) have attracted much attention due to their high power density and rapid response [3]. Conventionally a battery bank consisting of series-parallel modules (to build up the necessary voltage and current ratings) is connected to a grid-tied inverter through a bidirectional step-up dc-dc converter [2], [4]. Most commonly, the grid-tied inverter is a two-level (2L) or three-level (3L) voltage source converter (VSC) [1]. However, to rectify the drawbacks of these topologies, e.g., uneven voltage distribution and uneven charging/discharging currents caused by long battery strings, integration of BESS into the sub-modules of modular multilevel converters (MMCs) has been explored as a viable and enhanced alternative [1], [2]. In this topology, the batteries are distributed among the sub-modules, thus allowing the use of small battery strings with better control of their state-of-charge. Despite its advantages, this topology requires a dc-dc converter in each sub-module, which adds to its complexity. Given the numerous design and operating parameters that affect both classes of converter, estimation of their losses is a complicated problem. Estimation of converter losses is important prior to designing thermal management and protection schemes [5], [6], [7]. According to the loss comparisons available in literature [5], [8], a 2L VSC has higher converter losses than a conventional MMC. However, with the integration of BESSs, the losses change due to the additional semiconductor devices. Thus, this paper aims to evaluate the semiconductor losses of 2L VSC and MMC topologies with different BESS configurations.

This paper considers a regular MMC augmented with a conventional BESS (MMC-BESS), an MMC with embedded BESS in every sub-module (MMC-Full-ES), an MMC with embedded BESS in some of the sub-modules (MMC-Partial-ES), and a 2L VSC with a conventional BESS (2L-VSC-BESS). Regardless of the configuration, all topologies are designed to deliver the same amount of power. The test systems are modeled in an EMT simulation program (PSCAD/EMTDC) using detailed or detailed equivalent models and a simulation-based loss calculation approach [9] is used to externally determine their losses by utilizing voltage, current, and switching waveforms obtained from the EMT simulator. The paper focuses only on the semiconductor losses, and does not discuss the losses in the transformer or other passive elements. The impacts of the dc-dc converter frequency and also the circulating current suppression controller (CCSC) of MMC topologies on the losses are investigated. Semiconductor losses associated with the topologies are compared and analyzed thoroughly.

II. Simulation-Based Loss Calculation Method

Semiconductor losses primarily include conduction, off-state, and switching losses. Conduction losses are the product of the device current and on-state voltage. Methods using either a constant on-state voltage (i.e., forward saturation voltage) ([6], [7]) or a collector current-dependent on-state voltage ([10], [11], [12]) exist in contemporary literature. Similarly, off-state losses are the product of the off-state voltage and the leakage current and are essentially negligible. Calculation of switching losses, however, is not straightforward due to the small turn-on and turn-off transients, and requires sophisticated methods. Analytical [10], [11] and simulation-based [5], [7], [13] methods have been used to estimate switching losses. Due to the complexity of the switching patterns of power electronic converters and

This work was supported the University of Manitoba, the Natural Sciences and Engineering Research Council (NSERC) of Canada, Manitoba Hydro, and MITACS. D. Kuranage and S. Filizadeh are with the University of Manitoba, Winnipeg, MB, Canada (e-mail of corresponding author: shaahin.filizadeh@umanitoba.ca). I. Fernando is with Manitoba Hydro, Winnipeg, MB, Canada (e-mail: itfernando@hydro.mb.ca).

Paper submitted to the International Conference on Power Systems Transients (IPST2025) in Guadalajara, Mexico, June 8-12, 2025.

the often large number of switching devices included in them, it is convenient to use a simulation-based approach to calculate their losses. However, most existing simulation-based methods, e.g., [5], [7], and [13], utilize complex equations, are time-consuming, and add significant time to the already strained EMT simulation time of converters.

The approach used in this paper is adopted from the authors' recent work [9] and estimates the switching losses considering pre- and post-switching currents and voltages obtained from the EMT simulation waveforms. This method achieves computational efficiency by avoiding run-time loss calculations. Instead, losses are calculated using post-processing of simulation data following the completion of the EMT solution. Detailed comparative assessments against other loss assessment methods as well as experimental results are reported in [9] and confirm the accuracy of this method. In this method, explicit expressions for different loss components are fitted to energy loss curves from device data sheets. EMT simulation results are then used to explicitly evaluate energy losses for all switching events and conduction periods using point-on-wave data; they are then tallied to determine converter losses over a given interval.

The turn-on ($E_{\rm on}$), turn-off ($E_{\rm off}$), and diode reverse recovery ($E_{\rm rr}$) energy losses are of the following forms:

$$E_{\rm on} = E_{{\rm on},T^\circ{\rm C}}(I_{\rm c}) \cdot K_{\rm V} \tag{1}$$

$$E_{\rm off} = E_{{\rm off},T^\circ{\rm C}}(I_{\rm c}) \cdot K_{\rm V} \tag{2}$$

$$E_{\rm rr} = E_{{\rm rr},T^\circ{\rm C}}(I_{\rm c}) \cdot K_{\rm V} \tag{3}$$

$$K_{\rm V} = \frac{V_{\rm ce}}{V_{\rm test}} \tag{4}$$

where $I_{\rm c}$ is the device current and $E_{{\rm on},T^\circ{\rm C}}(I_{\rm c})$, $E_{{\rm off},T^\circ{\rm C}}(I_{\rm c})$, and $E_{{\rm rr},T^\circ{\rm C}}(I_{\rm c})$ are turn-on, turn-off, and diode reverse recovery energy losses, respectively, and are expressed as a function of the device current at the switching instant. Off-state blocking losses are generally negligible. Device data sheet curves, which are used in curve fitting to obtain $E_{{\rm on},T^\circ{\rm C}}(I_{\rm c})$, $E_{{\rm off},T^\circ{\rm C}}(I_{\rm c})$, and $E_{{\rm rr},T^\circ{\rm C}}(I_{\rm c})$, are often given for a certain collector-emitter voltage ($V_{\rm test}$). For other collector-emitter voltage ($V_{\rm ce}$) values, which occur during operation, a correction factor ($K_{\rm V}$) must be applied. The method used in this paper is based upon a proportional relationship with the voltage as shown in (4). This is shown, through extensive assessment, to be a reasonable assumption with minimal impact on accuracy [9]. For a conservative estimation of losses, maximum permissible junction temperature is assumed.

The IGBT-diode pair used in this paper is ST1500GXH24, rated at 4.5 kV and 1.5 kA, although any other suitable device may be readily used. Table I shows the equations fitted to the data sheet energy loss curves of this device, as well as other parameters needed to calculate losses. The losses are calculated offline, i.e., using the EMT simulation results of the converter as described in [9]. Note that EMT models of switches normally do not include a large amount of device-specific details; the proposed method does not need any changes to device models within the simulator. The voltage, current, and switching function waveforms of the semiconductor devices after the converter settles into steady

TABLE I
EQUATIONS FITTED TO DATA SHEET CURVES OF ST1500GXH24 AT 125°C AND OTHER PARAMETERS REQUIRED FOR LOSS ESTIMATION

Equations fitted to the data sheet curves	
$E_{{\rm on},125^\circ{\rm C}}(I_{\rm c})$	0.0051 $I_{\rm c}$ + 0.4885
$E_{{\rm off},125^\circ{\rm C}}(I_{\rm c})$	$6 \times 10^{-7} I_{\rm c}^2$ + 0.0034$I_{\rm c}$ + 0.5916
$E_{{\rm rr},125^\circ{\rm C}}(I_{\rm c})$	$-1 \times 10^{-7} I_{\rm c}^2$ + 0.0021$I_{\rm c}$ + 0.5315
Data sheet parameters	
On-state voltage	IGBT = 3 V Diode = 3.2 V
Voltage at test condition	2.7 kV

state are used as the inputs to the loss calculation algorithm. Changes in the switching state of a device (from 0 (OFF) to 1 (ON) or vice versa) in two consecutive time steps are used to detect switching events. The direction of the current at that moment determines the turning-on and turning-off diode or IGBT. Subsequently, the algorithm adds the required $E_{\rm on}$, $E_{\rm off}$, or $E_{\rm rr}$. Conduction losses are calculated by multiplying the device current by its on-state voltage during conduction and are tallied separately. In this paper a constant on-state voltage (i.e., forward saturation voltage) [6], [7] is used due to its simplicity of implementation while maintaining a high degree of accuracy. In the simulation-based studies shown in Section III, energy losses are calculated for a 1-second period in steady state and for one phase of the topologies considered. The obtained losses are then multiplied by 3 to obtain the three-phase converter's entire semiconductor losses.

III. BESS CONVERTER TOPOLOGIES

The general layout of the system considered is shown in Fig. 1. Several converter topologies, as shown in Fig. 2, are used to connect the external dc system (see points A and B in Fig. 1) to the ensuing ac system. The BESS topologies in Fig. 2 include templates based upon conventional 2L VSC and MMC schemes, and are simulated in PSCAD/EMTDC using detailed switching or detailed equivalent models that fully consider all switching events for all semiconductor devices. General specifications of the system are given in Table II.

A. MMC-Based Topologies

Three MMC-based topologies are considered as depicted in Fig. 2: (i) MMC-BESS is a conventional MMC with

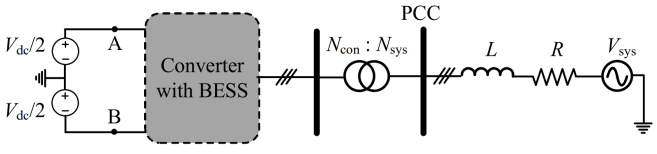

Fig. 1. Schematic diagram of the system under consideration.

TABLE II
GENERAL SYSTEM SPECIFICATIONS

Parameter	Value
Dc voltage ($V_{\rm dc}$)	45 kV
Ac grid voltage ($V_{\rm sys}$)	20.9 kV SCR =3 $\angle 80^\circ$
Transformer ratio ($N_{\rm con}$:$N_{\rm sys}$)	26.18 : 20.9 kV
Transformer rating and reactance	54 MVA 6 %
Network side impedance ($R + {\rm j}X$)	0.561+j3.185 Ω

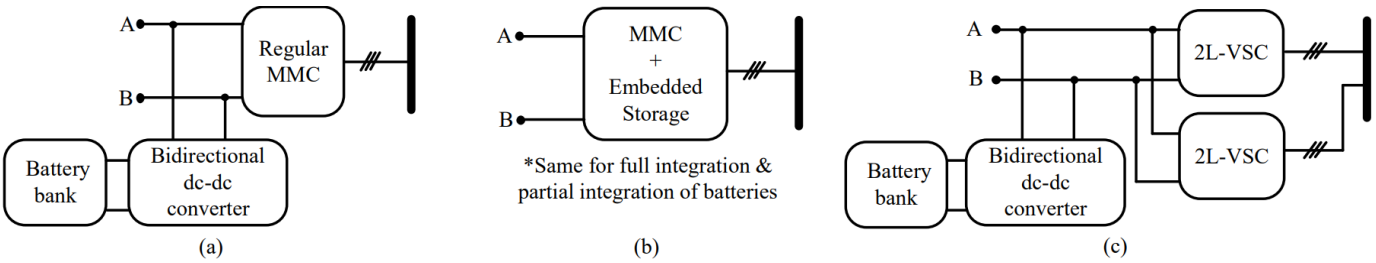

Fig. 2. Schematic diagrams of the converter and BESS connections, (a) MMC-BESS, (b) MMC-Full-ES / MMC-Partial-ES, (c) 2L-VSC-BESS.

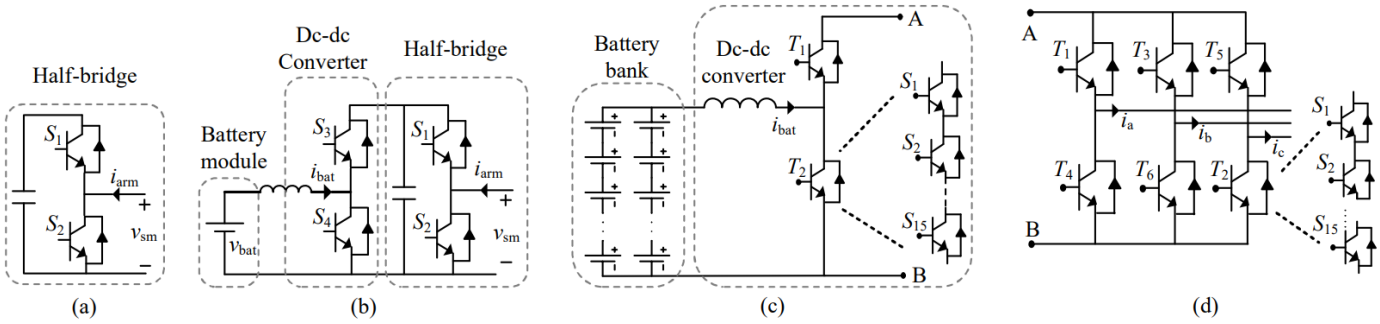

Fig. 3. Converter sub-systems: (a) A regular half-bridge sub-module, (b) sub-module with embedded storage (SM-ES), (c) battery bank and bidirectional dc-dc converter, (d) a two-level voltage source converter.

half-bridge sub-modules (see Fig. 3(a)); the batteries are connected to the dc-side of the MMC using a bi-directional dc-dc converter (see Fig. 3(c)); (ii) MMC-Full-ES uses small battery packs connected to individual sub-modules via a dc-dc converter (see Fig. 3(b)); and (iii) MMC-Partial-ES has a similar structure to MMC-Full-ES except that the batteries are connected to a subset of sub-modules while the remaining ones are regular sub-modules. The ac-side controls are the same for all topologies. Conventional sorting and balancing [2] is used for inserting and bypassing sub-modules. Battery currents are controlled using the peak current control technique [14].

1) MMC-BESS: In this topology, an MMC with regular sub-modules is connected to a conventional BESS using a bidirectional dc-dc converter. In the simulations in this paper, the battery bank includes 120 batteries in 6 strings of 20 battery modules of 0.8 kV in series to build up to 16 kV (see the second row of Table III). T_1 and T_2 in Fig. 3(c) represent valve groups of 15 IGBT-diode pairs in series. Hence the valve group has a dc voltage blocking capability of 67.5 kV, which is higher than the 45 kV dc-side voltage with an over-voltage safety margin. The rated power of the battery bank is 9.6 MW (16 kV$\times$0.6 kA). This topology includes 240 and 30 IGBT-diode switches in half-bridges and dc-dc converter, respectively.

2) MMC-Full-ES: All the sub-modules in this topology include a small battery pack and a dc-dc converter totaling 120 batteries of 0.8 kV each. The total rated power of the batteries is 9.6 MW (0.8 kV$\times$0.1 kA$\times$20$\times$6). Detailed specifications of this system are given in the third row of Table III. There are 240 IGBT-diode modules in half-bridges and 240 IGBT-diode modules in dc-dc converters.

3) MMC-Partial-ES: In this configuration, half of the sub-modules in the multivalve are regular sub-modules (Fig. 3(a)), and the rest are sub-modules with embedded storage (Fig. 3(b)). The converter is connected to the grid similar to MMC-Full-ES (Fig. 2(b)). Other details of this topology are given in the fourth row of Table III. The sub-modules with embedded storage include 2 batteries of 0.8 kV each in parallel to increase their current capability. The rated power of the batteries is 9.6 MW (0.8 kV$\times$0.2 kA$\times$10$\times$6). This topology includes 240 and 120 IGBT-diode switches in half-bridges and dc-dc converters, respectively.

B. Two-Level VSC BESS Topology

This topology is shown in Fig. 2(c). Since the rated current of the selected IGBT-diode module is 1.5 kA, two 2L VSCs are connected in parallel to deliver the same amount of power as the other topologies. Fig. 3(d) illustrates the design of a 2L VSC. T_1, T_2, T_3, T_4, T_5, and T_6 represent strings of 15 IGBT-diode modules in series to build up their total dc-voltage blocking ability. Sinusoidal pulse width modulation (SPWM) technique is used to generate switching signals. The two VSCs include 180 IGBT-diode modules and the dc-dc converter includes 30 of them.

IV. Simulation Results

Decoupled control (for inverters) and peak current control (for batteries) are used to adjust active power ($P_{\mathrm{PCC,ref}}$) and voltage magnitude ($V_{\mathrm{PCC,ref}}$) at the point of common coupling (PCC), and battery currents ($i_{\mathrm{bat,ref}}$), respectively. Six operating points are considered by changing the reference values as in Table IV. To deliver the same amount of power from the batteries regardless of the converter topology,

TABLE III
SPECIFICATIONS OF THE MMC-BASED TOPOLOGIES

Topology	No of sub-modules per multivalve		Sub-module capacitor		Dc-dc converter inductance	BESS specifications	
	Regular SMs	SM-ES	Capacitance	Voltage		Battery voltage	Max/min battery current
MMC-BESS	20	0	8000 μF	2.25 kV	0.6 H	16 kV (20×0.8 kV)	$\pm$ 0.6 kA
MMC-Full-ES	0	20	8000 μF	2.25 kV	0.1 H	0.8 kV (1×0.8 kV)	$\pm$ 0.1 kA
MMC-Partial-ES	10	10	8000 μF	2.25 kV	0.1 H	0.8 kV (1×0.8 kV)	$\pm$ 0.2 kA

* Regular SMs and SM-ES refer to regular sub-modules and sub-modules with energy storage, respectively.

TABLE IV
OPERATING POINTS CONSIDERED IN THE STUDY

Parameters		Operating points					
		1	2	3	4	5	6
$V_{\mathrm{PCC,ref}}$ (pu)		1	1	1	1	1	1
$P_{\mathrm{PCC,ref}}$ (pu)		0.9	0.9	0.9	0.8	0.8	0.8
$i_{\mathrm{bat,ref}}$* (kA)	MMC-BESS	0	0.6	-0.6	0	0.6	-0.6
	MMC-Full-ES	0	0.1	-0.1	0	0.1	-0.1
	MMC-Partial-ES	0	0.2	-0.2	0	0.2	-0.2
	2L-VSC_BESS	0	0.6	-0.6	0	0.6	-0.6

* Positive direction of $i_{\mathrm{bat,ref}}$ is as shown in Fig. 3(b) and (c).

different battery current references are needed. The impact of dc-dc converter frequency and the MMC's circulating current suppression controller (CCSC) on the converter losses are investigated for all considered operating points in Table IV. The operating points include charging and discharging cases at two power flow values out of the converters.

A. Effect of DC-DC Converter Frequency

For MMC topologies, dc-dc converter frequency is set to 1000 Hz, 1500 Hz, and 2000 Hz and total semiconductor losses are estimated while CCSC is activated. In the 2L-VSC-BESS topology, significantly higher losses are recorded even at 1000 Hz (see Fig. 4(l)), rendering the other two dc-dc converter frequencies impractical for this topology. SPWM carrier frequencies of 900 Hz and 1260 Hz are used, while maintaining dc-dc converter frequency at 1000 Hz. The loss percentages are calculated by taking the percentage of total losses over active power injection (in MWs) of every operating point.

1) MMC-BESS loss analysis: As seen in Fig. 4(a), losses related to the half-bridges remain the same for all dc-dc converter frequencies as they are not affected by that frequency. For the same $P_{\mathrm{PCC,ref}}$ value, the arm current is the same despite the variations of the battery current. Thus operating points 1, 2, and 3 have equal losses. The same applies to operating points 4, 5, and 6. The losses in the dc-dc converter increase with its switching frequency (Fig. 4(b)). When $i_{\mathrm{bat,ref}}$ is zero (operating points 1 and 4), losses are low but not zero due to the operation of peak current controller. Since the magnitude of $i_{\mathrm{bat,ref}}$ is equal in operating points 2 and 3, the losses at those points are nearly equal when identical switching frequencies are used. They are, however, not exactly the same since the magnitude of the actual average battery current is slightly lower and higher than the reference value when it is positive and negative, respectively, due to the operation of peak current controller. Operating points 5 and 6 also have approximately equal losses for the same reason.

Fig. 5 shows the losses separated into conduction and switching. As seen in Figs. 5(a)-(b), conduction losses remain the same for all dc-dc converter frequencies while switching losses increase with the frequency. The switching losses are almost twice as much as conduction losses. Compared with other topologies, Fig. 6 shows that this converter topology has the lowest total losses, in the range of 1.1% to 1.6% (Fig. 4(c)). However, due to the disadvantages associated with the conventional BESS, this topology is not suitable for high voltage systems.

2) MMC-Full-ES loss analysis: Fig. 4(d) shows the losses in the half-bridges of MMC-Full-ES. As mentioned earlier, the dc-dc converter frequency bears no impact on the operation of half-bridges. However, in this topology, operating points 1, 2, and 3 have different arm currents even though they have the same $P_{\mathrm{PCC,ref}}$, due to the different battery currents. The total power that must be delivered to the ac side is the addition of the power that is supplied from the dc side and the batteries. When the battery current is positive (operating point 2), batteries supply part of the total power, reducing the dc-side power and decreasing the dc component of the arm current. In contrast, when the battery current is negative (operating point 3), batteries are charging; hence the dc side supplies power to both the ac side and the batteries. Therefore, the arm current includes a large dc component. When the battery current is zero, the dc side supplies the total power for the ac side so that the dc component of the arm current lies in between the values of operating points 2 and 3. Fig. 7 shows the arm currents for operating points 1, 2, and 3 when the dc-dc converter frequency is 1000 Hz and CCSC is active. The same applies to the operating points 4, 5, and 6.

As in Fig. 4(e), losses associated with the dc-dc converters increase with the increasing frequency, although they are significantly lower than the losses in the half-bridges since the battery current is around one-tenth of the peak arm current. Besides, dc-dc converter losses in this topology are slightly higher than those in MMC-BESS and MMC-Partial-ES topologies, due to the larger number of semiconductor devices present in the dc-dc converters. The conduction and switching losses of this converter topology versus the dc-dc converter frequency are displayed in Figs. 5(c) and (d). Around 70%-75% of the total converter losses are due to switching. This converter topology has the second highest total losses, which range from around 1.3% to 2.2% (Fig. 4(f)). Since all the sub-modules are augmented with batteries, more semiconductor devices are utilized. Nevertheless, this topology is suited for both high- and medium-voltage systems since the batteries are embedded into the sub-modules.

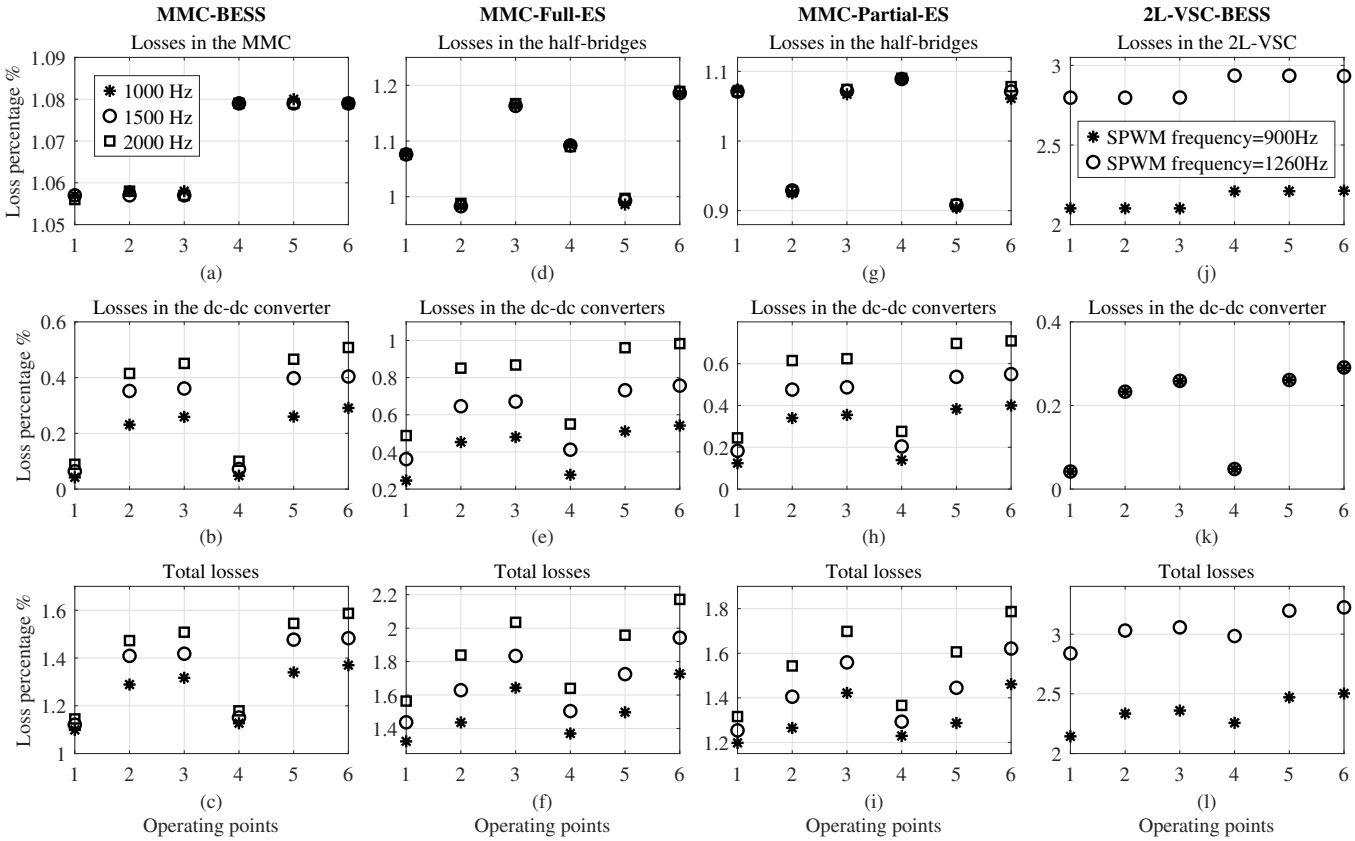

Fig. 4. Loss analysis of the 4 topologies with different dc-dc converter frequencies (CCSC is on for MMC topologies),(a)(b)(c) Loss analysis of MMC-BESS, (d)(e)(f) Loss analysis of MMC-Full-ES, (g)(h)(i) Loss analysis of MMC-Partial-ES, (j)(k)(l) Loss analysis for 2L-VSC-BESS.

3) MMC-Partial-ES loss analysis: Fig. 4(g) illustrates the losses associated with the half-bridges of MMC-Partial-ES. This topology includes both the regular sub-modules and sub-modules with embedded storage. Only the arm current flows through the capacitors in the regular sub-modules while those in the sub-modules with batteries are exposed to both the battery and arm currents. Thus, the capacitor voltage balancing algorithm treats these two types of sub-modules differently.

Since the power reference ($P_{\mathrm{PCC,ref}}$) of the converter is positive, the arm current is primarily in the charging direction. Hence, the capacitor voltage balancing algorithm inserts the capacitors with the lowest voltages more frequently. When the battery current is positive, it charges the capacitor voltage, so that the capacitors in sub-modules with batteries are not frequently inserted. Therefore, the switching losses are lower in sub-modules with embedded BESS with respect to the regular sub-modules when the battery current is in the positive direction. This effect reverses when the battery current becomes negative. Fig. 8 shows the comparison of average number of switching events in the upper switch of the half-bridge part of the two types of sub-modules for one second when the dc-dc converter frequency is 2000 Hz and CCSC is active.

Even though the battery current is higher, the losses of the dc-dc converters in this topology are lower than in MMC-Full-ES as displayed in Fig. 4(h), due to fewer switching devices utilized in this topology. The conduction losses (Fig. 5(e)) are almost the same as in MMC-Full-ES, while the switching losses (Fig. 5(f)) are lower than that of MMC-Full-ES. According to the total loss comparison in Fig. 6, this topology has the second lowest losses ranging from approximately 1.2% to 1.8% (Fig. 4(i)). Higher battery currents result in higher losses while fewer switching devices reduce the losses. Hence, by selecting the number of normal sub-modules and sub-modules with embedded storage in an optimal way one can make a significant reduction in converter losses. Moreover, this topology can be used in both high- and medium-voltage systems.

4) 2L-VSC-BESS loss analysis: This topology has the highest losses among the considered topologies, which vary between approximately 2.1% -3.3% (Fig. 4(l)). The high SPWM switching frequency is the main reason for these higher losses. When the SPWM frequency is changed from 900 Hz to 1260 Hz, there is an increase of about 0.7% in losses as shown in Fig. 4(j). The same results appear in the analysis of conduction and switching losses in Figs. 5(g) and (h). Since the SPWM frequency does not impact the dc-dc converter operation, the losses of the conventional BESS remains the same and lie around 0.04% - 0.3% (Fig. 4(k)). Even though the loss analysis results with the changing dc-dc converter frequency are not shown for this case, they are the same as the losses of dc-dc converter in MMC-BESS as in Fig. 4(b), since the converters and the BESS unit are working separately in MMC-BESS and 2L-VSC-BESS topologies. Besides, this

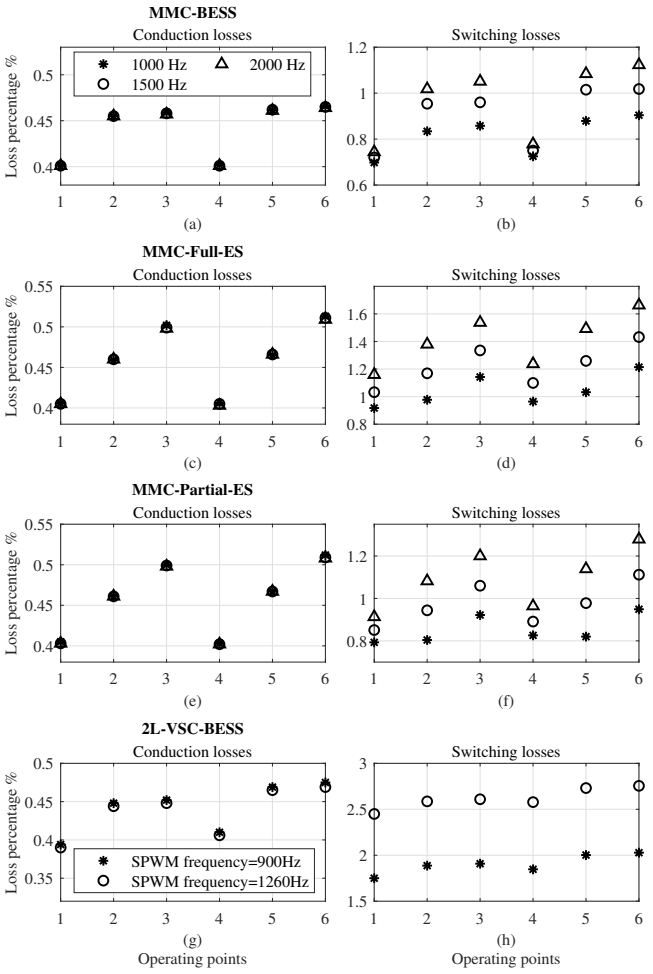

Fig. 5. Switching and conduction loss percentages of the 4 topologies with different dc-dc converter frequencies (CCSC is on for MMC topologies), (a) conduction, (b) switching losses in MMC-BESS, (c) conduction, (d) switching losses in MMC-Full-ES, (e) conduction, (f) switching losses in MMC-Partial-ES, (g) conduction, (h) switching losses in 2L-VSC-BESS.

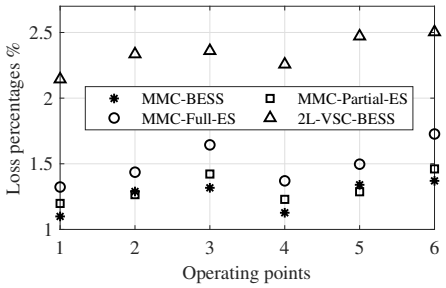

Fig. 6. Total loss comparison for dc-dc converter frequency of 1000 Hz; CCSC is on (SPWM frequency for 2L-VSC = 900 Hz).

topology is suitable only for medium voltage systems due to its 2L arrangement.

B. Effect of CCSC Operation

Fig. 9 shows the loss estimation only for MMC topologies with and without the CCSC operation when the dc-dc converter frequency is 2000 Hz. CCSC eliminates the second-harmonic component from the arm current, reducing

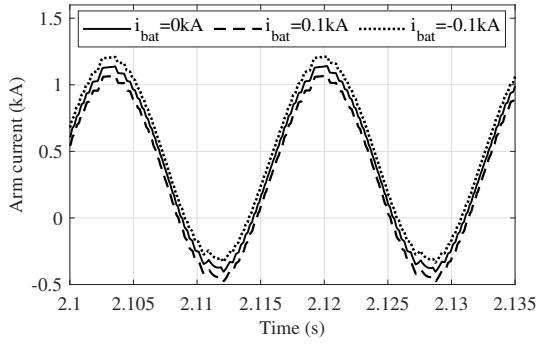

Fig. 7. Upper arm currents of phase a for 1 ($i_{\mathrm{bat,ref}}$=0 kA), 2 ($i_{\mathrm{bat,ref}}$=0.1 kA), and 3 ($i_{\mathrm{bat,ref}}$=-0.1 kA) operating points when dc-dc converter frequency is 1000 Hz and CCSC is in operation.

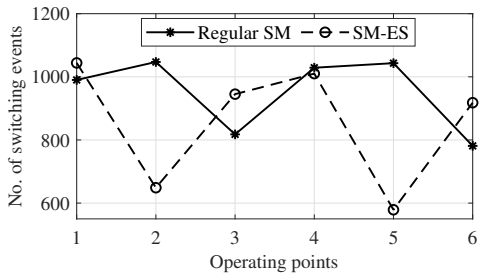

Fig. 8. Average switching events in a regular sub-module (regular SM) and sub-module with embedded BESS (SM-ES) for 1-second period when the dc-dc converter frequency is 2000 Hz and CCSC is on.

the converter losses significantly. Besides, when the circulating currents are suppressed, the arm current fluctuates less, leading to lower changes in the capacitor voltages, and lower switching events in the sub-modules. Fig. 10 displays the comparison of average switching events of half-bridge portion of a sub-module for a 1-second period with and without the CCSC for MMC-Full-ES and MMC-Partial-ES topologies. There is a loss reduction of about 0.23% in MMC-BESS and 0.3% in MMC-Full-ES when the CCSC is activated. In MMC-Partial-ES, losses are reduced by approximately 0.31%-0.36% depending on the operating point, while CCSC is active. A high-level summery of losses in MMC topologies is displayed in Table V. The table shows how the losses change within a topology with the battery current.

V. The Effect of Temperature on Losses

Junction temperature is an important factor in calculating losses. However, considering its impact on semiconductor losses requires sophisticated thermal models that must include the cooling conditions of the converter to determine the junction temperature as a function of the device current. Moreover, semiconductor device datasheets provided by manufacturers only give energy loss curves for few operating temperatures. Hence, estimation of the losses as the temperature changes requires many assumptions about a wide range of physical phenomena (e.g., converter and sub-module layout, cooling systems, etc.), which will adversely affect the accuracy and reliability of the estimated loss figures.

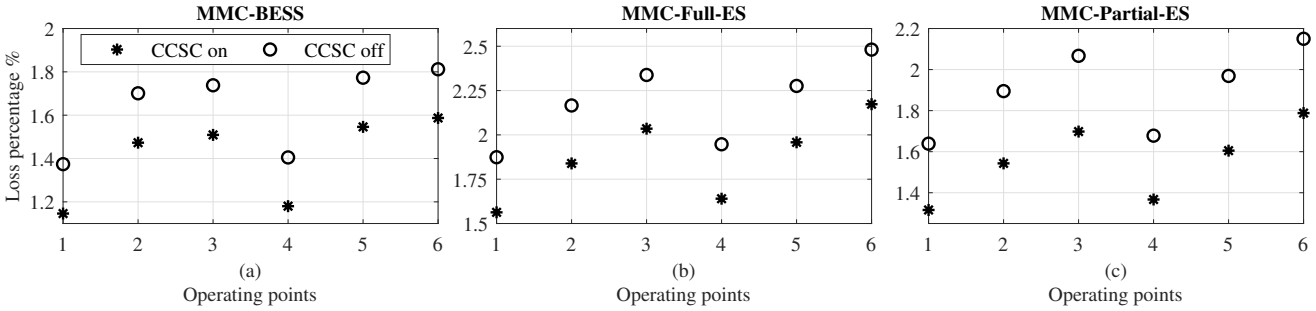

Fig. 9. Loss analysis with and without CCSC operation (dc-dc converter frequency = 2000 Hz), (a) losses in MMC-BESS, (b) losses in MMC-Full-ES, (c) losses in MMC-Partial-ES.

TABLE V
SUMMERY OF THE LOSS ANALYSIS OF MMC TOPOLOGIES[1]

Topology[2]	i_{bat}	Losses	Suitability for HV systems
MMC-BESS	Charging	High and nearly equal	No
	Discharging		
	0	Low	
MMC-Partial-ES	Charging	High	Yes
	Discharging	Medium	
	0	Low	
MMC-Full-ES	Charging	High	Yes
	Discharging	Medium	
	0	Low	

[1]Concluded for positive P_{ref} and both CCSC on and off conditions.
[2]Converters in ascending order in terms of semiconductor losses.

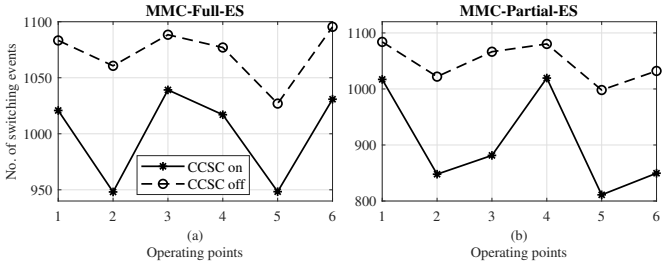

Fig. 10. Average switching events of one sub-module (half-bridge portion) within one second with and without CCSC (dc-dc converter frequency = 2000 Hz), (a) for MMC-Full-ES, (b) for MMC-Partial-ES.

The method used in this paper is based upon the worst-case scenario of operating at the maximum permissible junction temperature (i.e., 125 °C). In this section loss estimations for operating at a low temperature of 25 °C, for which the datasheet curves are available are presented. Loss estimation equations (see Table VI) are fitted to these curves. Estimated losses at these two operating temperatures provide upper and lower bands without calculating junction temperature as the device current varies and circumvents development and tuning a thermal model for which parameters are prohibitively difficult to find. A sample of losses at 25 °C for MMC-Full-ES when dc-dc converter frequency is 2000 Hz are displayed in Table VII, which also show the ranges over which the losses are expected to change depending on the temperature.

TABLE VI
EQUATIONS FITTED TO DATA SHEET CURVES OF ST1500GXH24 AT 25 °C AND OTHER PARAMETERS REQUIRED FOR LOSS ESTIMATION

Equations fitted to the data sheet curves	
$E_{\mathrm{on},25\,^\circ\mathrm{C}}(I_{\mathrm{c}})$	0.0039 I_{c} - 0.0589
$E_{\mathrm{off},25\,^\circ\mathrm{C}}(I_{\mathrm{c}})$	$5\times10^{-7}I_{\mathrm{c}}^2$ + 0.0023I_{c} - 0.1484
$E_{\mathrm{rr},25\,^\circ\mathrm{C}}(I_{\mathrm{c}})$	$-6\times10^{-8}I_{\mathrm{c}}^2$ + 0.0012I_{c} + 0.1001
Data sheet parameters	
On-state voltage	IGBT = 2.53 V Diode = 3 V

TABLE VII
LOSS COMPARISON OF MMC-FULL-ES FOR MINIMUM AND MAXIMUM TEMPERATURES

OP	Loss % (CCSC off)		% Diff.	Loss % (CCSC on)		% Diff.
	25 °C	125 °C		25 °C	125 °C	
1	1.019	1.874	0.855	0.778	1.563	0.785
2	1.189	2.166	0.976	0.941	1.839	0.898
3	1.313	2.338	1.025	1.079	2.035	0.956
4	1.011	1.947	0.936	0.776	1.64	0.865
5	1.205	2.276	1.071	0.963	1.958	0.995
6	1.350	2.481	1.131	1.114	2.173	1.059

*dc-dc converter frequency is 2000 Hz.

VI. CONCLUSIONS

The semiconductor losses of MMC-BESS, MMC-Full-ES, MMC-Partial-ES, and 2L-VSC-BESS topologies were evaluated using a simulation-based loss calculation approach, which uses current and voltage samples at the switching event to externally calculate the switching losses. Since the method uses post-processing of EMT simulation samples, it does not add to the time required for converter simulations. Neither does it require any sophisticated switch models to be developed for EMT solutions. The impact of dc-dc converter frequency and CCSC operation (only for MMC topologies) on converter losses were studied for different operating points. The analysis showed the MMC-BESS topology has the lowest losses ranging from approximately 1.1%-1.6%. MMC-Partial-ES has the second lowest losses in the range of 1.2%-1.8%. By properly selecting the number of regular sub-modules and those with embedded BESS, the losses of this topology can be significantly reduced. MMC-Full-ES has the second highest losses ranging from 1.3%-2.2%. 2L-VSC-BESS topology shows the highest losses (2.1%-3.3%). According to the battery currents, the arm currents in MMC-Full-ES and MMC-Partial-ES

topologies change resulting in different losses. When CCSC is active, the second-harmonic component is eliminated, lowering the switching events and the losses in the MMC topologies. The impact of temperature was exemplified by evaluating losses at minimum junction temperature for the MMC-Full-ES. Moreover, MMC-BESS and 2L-VSC-BESS topologies are not suitable for high-voltage systems due to their inherent voltage rating drawbacks, while MMC-Full-ES and MMC-Partial-ES topologies are suitable candidates for both high- and medium-voltage systems.

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